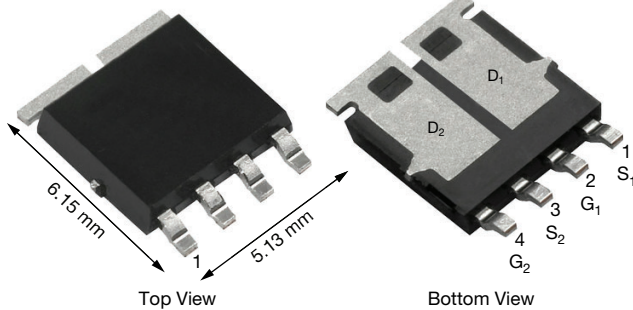


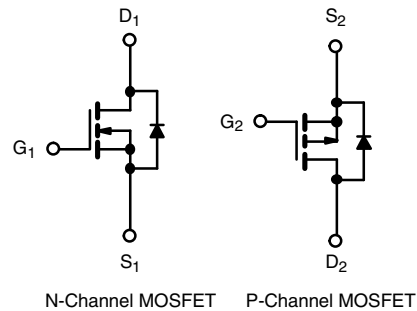
Automotive N- and P-Channel 100 V (D-S) 175 °C MOSFET

PowerPAK® SO-8L Dual


FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912

AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE


PRODUCT SUMMARY		
	N-CHANNEL	P-CHANNEL
V_{DS} (V)	100	-100
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 10$ V	0.0450	0.1460
$R_{DS(on)}$ (Ω) at $V_{GS} = \pm 4.5$ V	0.0580	0.2065
I_D (A)	15	-9.5
Configuration	N- and p-pair	

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SQJ570EP (for detailed order number please see www.vishay.com/doc?79771)

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain-source voltage		V _{DS}	100	-100	V
Gate-source voltage		V _{GS}	± 20		
Continuous drain current	T _C = 25 °C	I _D	15 ^a	-9.5	A
	T _C = 125 °C		9.6	-5.5	
Continuous source current (diode conduction) ^a		I _S	15	-15	
Pulsed drain current ^b		I _{DM}	40	-21	
Single pulse avalanche current	L = 0.1 mH	I _{AS}	13	-6	
Single pulse avalanche Energy		E _{AS}	8.4	1.8	mJ
Maximum power dissipation ^b	T _C = 25 °C	P _D	27	27	W
	T _C = 125 °C		9	9	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175		°C
Soldering recommendations (peak temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Junction-to-ambient	R_{thJA}	85	85	$^\circ\text{C/W}$
Junction-to-case (drain)	R_{thJC}	5.5	5.5	

Notes

- Package limited
- Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

**SPECIFICATIONS** ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		N-Ch	100	-	-	V
		V _{GS} = 0 V, I _D = -250 μA		P-Ch	-100	-	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		N-Ch	1.5	2	2.5	V
		V _{DS} = V _{GS} , I _D = -250 μA		P-Ch	-1.5	-2	-2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V		N-Ch	-	-	± 100	nA
				P-Ch	-	-	± 100	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 100 V	N-Ch	-	-	1	μA
		V _{GS} = 0 V	V _{DS} = -100 V	P-Ch	-	-	-1	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 125 °C	N-Ch	-	-	50	
		V _{GS} = 0 V	V _{DS} = -100 V, T _J = 125 °C	P-Ch	-	-	-50	
		V _{GS} = 0 V	V _{DS} = 100 V, T _J = 175 °C	N-Ch	-	-	150	
		V _{GS} = 0 V	V _{DS} = -100 V, T _J = 175 °C	P-Ch	-	-	-150	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	N-Ch	10	-	-	A
		V _{GS} = -10 V	V _{DS} ≤ 5 V	P-Ch	-6	-	-	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 6 A	N-Ch	-	0.0365	0.0450	Ω
		V _{GS} = -10 V	I _D = -6 A	P-Ch	-	0.1184	0.1460	
		V _{GS} = 10 V	I _D = 6 A, T _J = 125 °C	N-Ch	-	-	0.0774	
		V _{GS} = -10 V	I _D = -6 A, T _J = 125 °C	P-Ch	-	-	0.2435	
		V _{GS} = 10 V	I _D = 6 A, T _J = 175 °C	N-Ch	-	-	0.0978	
		V _{GS} = -10 V	I _D = -6 A, T _J = 175 °C	P-Ch	-	-	0.2994	
		V _{GS} = 4.5 V	I _D = 4 A	N-Ch	-	0.0468	0.0580	
		V _{GS} = -4.5 V	I _D = -4 A	P-Ch	-	0.1669	0.2065	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 6 A		N-Ch	-	15	-	S
		V _{DS} = -15 V, I _D = -6 A		P-Ch	-	7	-	
Dynamic ^b								
Input capacitance	C _{iss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	N-Ch	-	420	600	pF
		V _{GS} = 0 V	V _{DS} = -25 V, f = 1 MHz	P-Ch	-	480	650	
Output capacitance	C _{oss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	N-Ch	-	260	350	
		V _{GS} = 0 V	V _{DS} = -25 V, f = 1 MHz	P-Ch	-	250	350	
Reverse transfer capacitance	C _{rss}	V _{GS} = 0 V	V _{DS} = 25 V, f = 1 MHz	N-Ch	-	17	25	
		V _{GS} = 0 V	V _{DS} = -25 V, f = 1 MHz	P-Ch	-	20	30	
Total gate charge ^c	Q _g	V _{GS} = 10 V	V _{DS} = 50 V, I _D = 1 A	N-Ch	-	9	15	nC
		V _{GS} = -10 V	V _{DS} = -50 V, I _D = -1 A	P-Ch	-	12	20	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	V _{DS} = 50 V, I _D = 1 A	N-Ch	-	1.2	-	
		V _{GS} = -10 V	V _{DS} = -50 V, I _D = -1 A	P-Ch	-	2	-	
Gate-drain charge ^c	Q _{gd}	V _{GS} = 10 V	V _{DS} = 50 V, I _D = 1 A	N-Ch	-	1.9	-	
		V _{GS} = -10 V	V _{DS} = -50 V, I _D = -1 A	P-Ch	-	3	-	
Gate resistance	R _g	f = 1 MHz		N-Ch	1.3	2.7	4.5	Ω
				P-Ch	5	10.2	15.5	

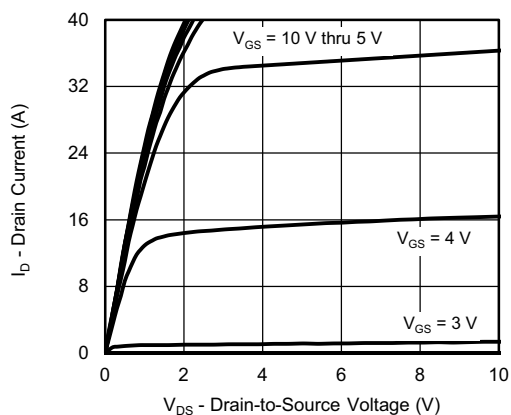
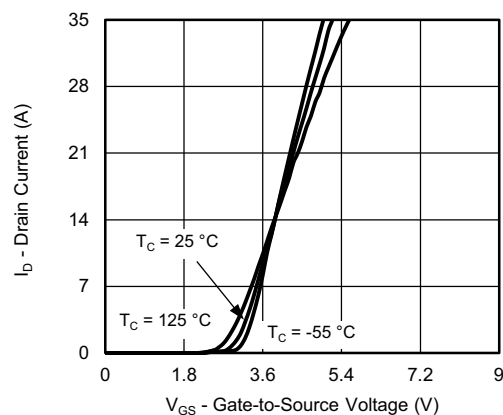
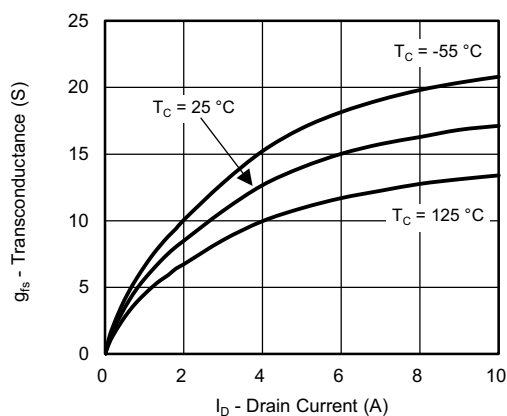
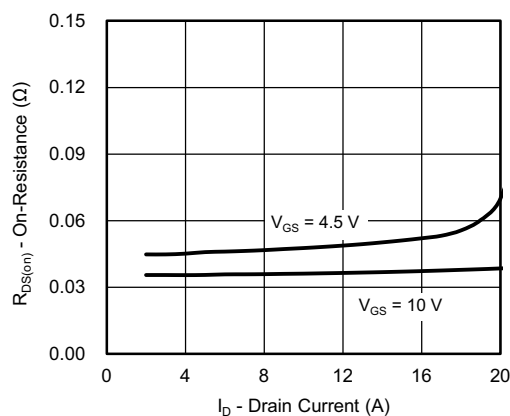
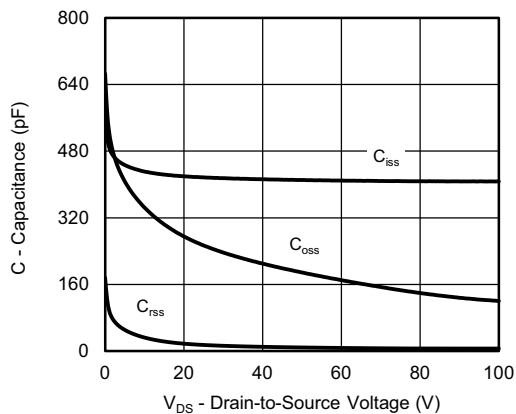
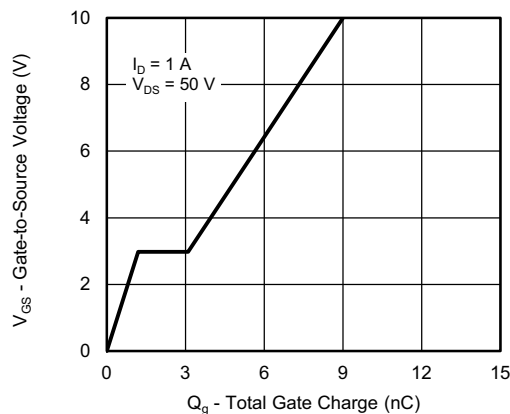


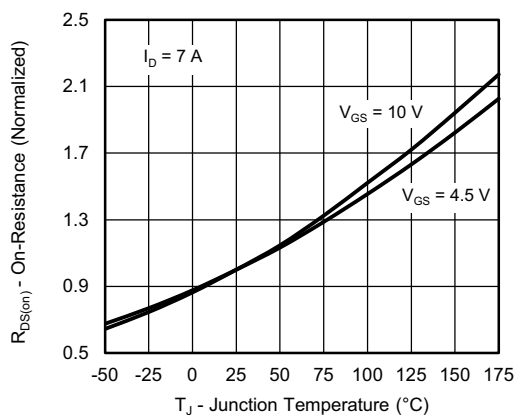
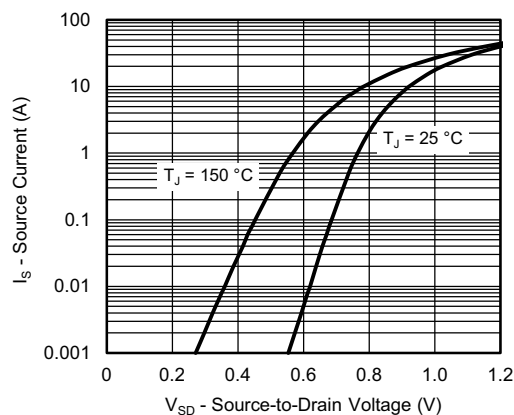
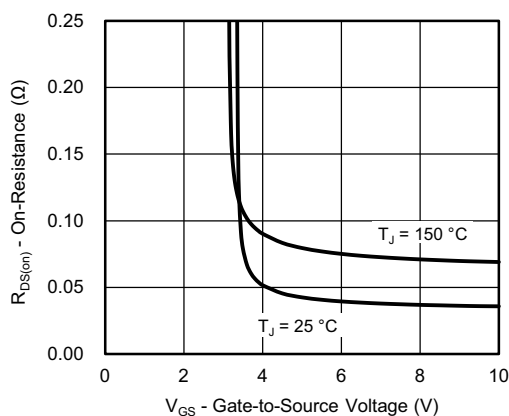
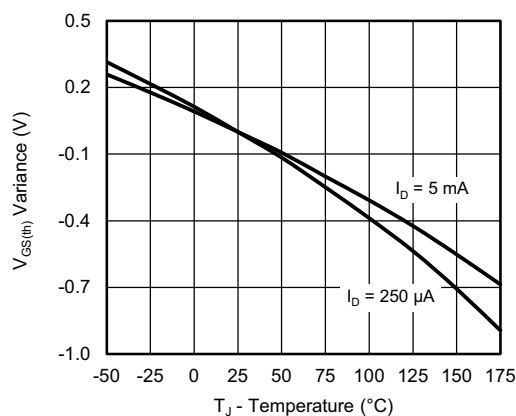
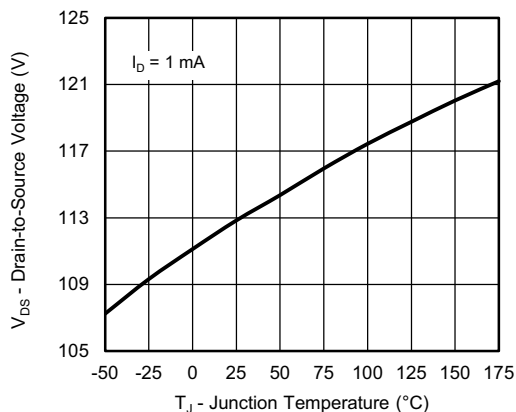
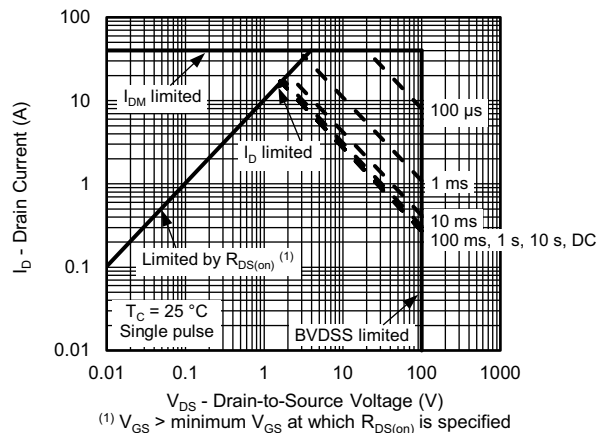
SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω, I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 5 Ω	N-Ch	-	8	15	ns
		V _{DD} = -50 V, R _L = 50 Ω, I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 5 Ω	P-Ch	-	12	20	
Rise time ^c	t _r	V _{DD} = 50 V, R _L = 50 Ω, I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 5 Ω	N-Ch	-	4	10	
		V _{DD} = -50 V, R _L = 50 Ω, I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 5 Ω	P-Ch	-	5	10	
Turn-off delay time ^c	t _{d(off)}	V _{DD} = 50 V, R _L = 50 Ω, I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 5 Ω	N-Ch	-	20	35	
		V _{DD} = -50 V, R _L = 50 Ω, I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 5 Ω	P-Ch	-	30	50	
Fall time ^c	t _f	V _{DD} = 50 V, R _L = 50 Ω, I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 5 Ω	N-Ch	-	17	30	
		V _{DD} = -50 V, R _L = 50 Ω, I _D ≅ -1 A, V _{GEN} = -10 V, R _g = 5 Ω	P-Ch	-	15	25	
Source-Drain Diode Ratings and Characteristics ^b							
Pulsed current ^a	I _{SM}		N-Ch	-	-	40	A
			P-Ch	-	-	-21	
Forward voltage	V _{SD}	I _S = 6 A	N-Ch	-	0.89	1.2	V
		I _S = -6 A	P-Ch	-	-0.89	-1.2	

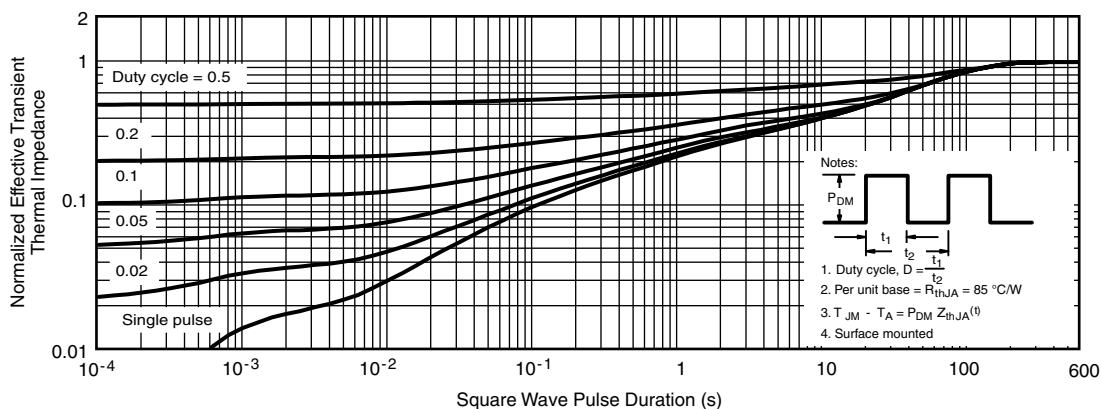
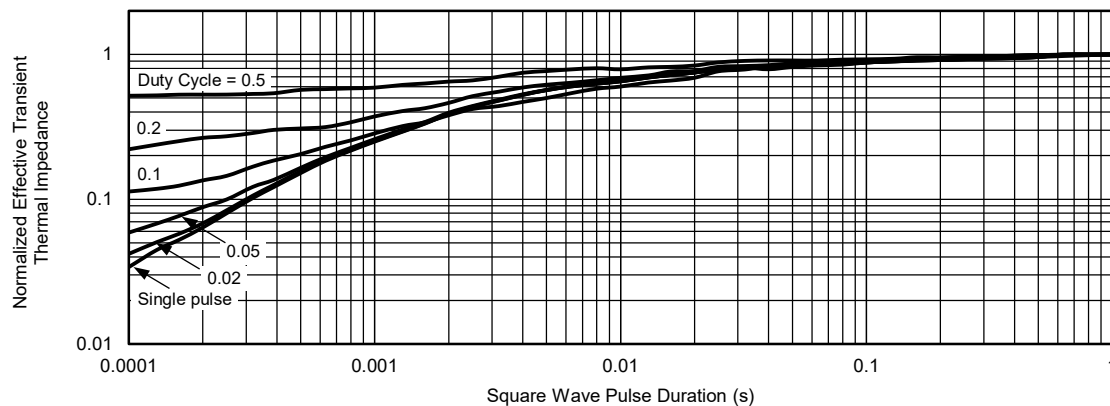
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

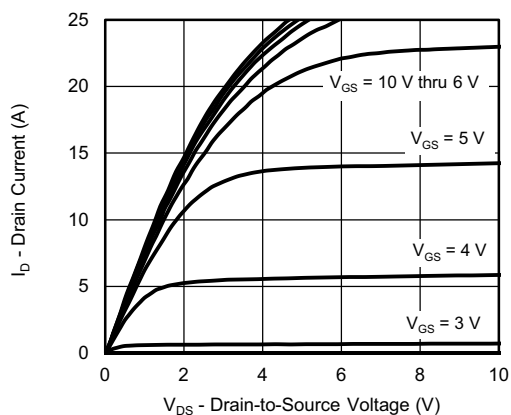
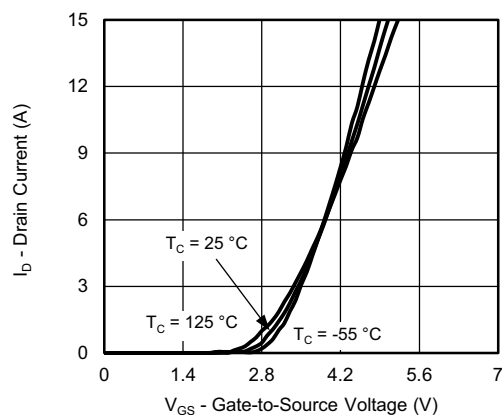
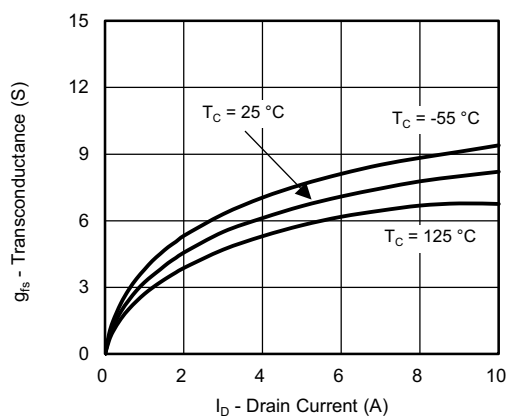
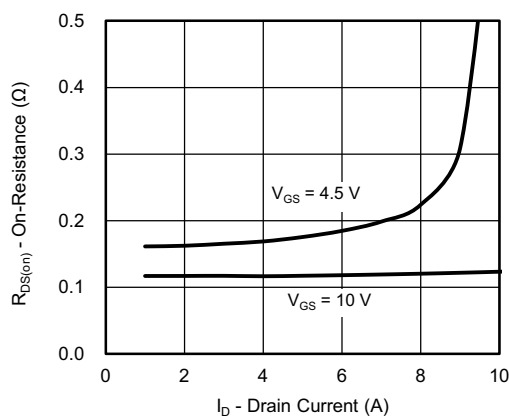
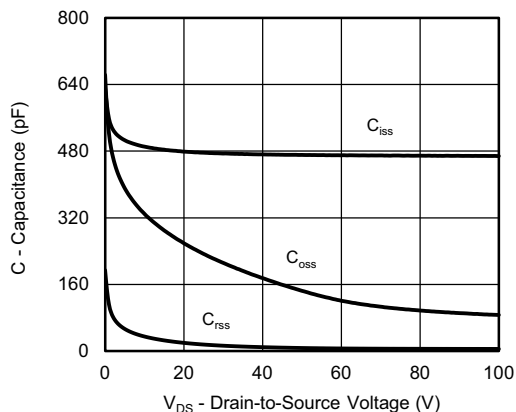
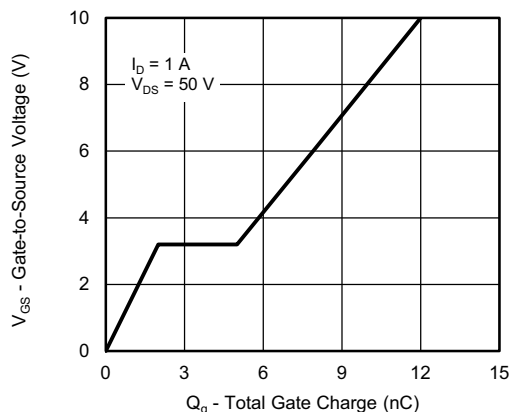
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

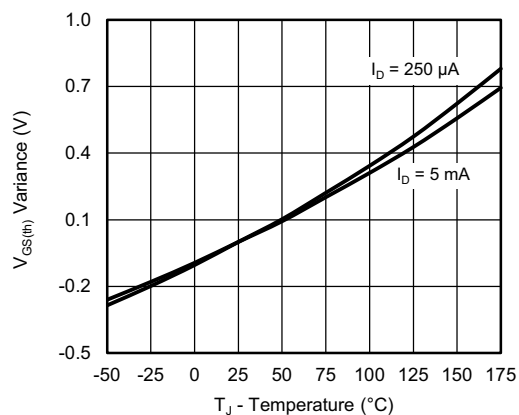
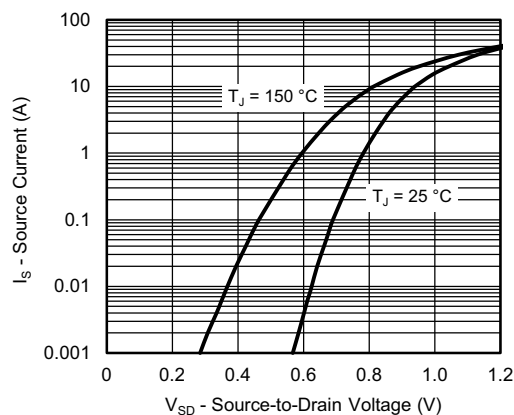
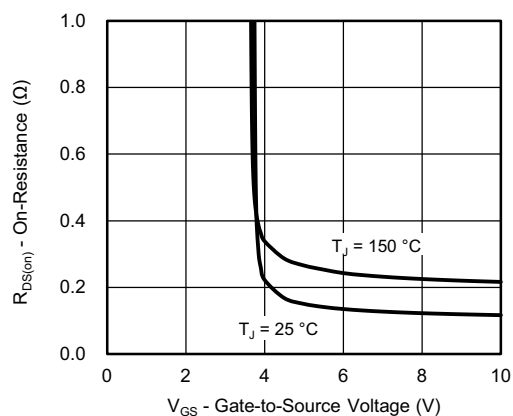
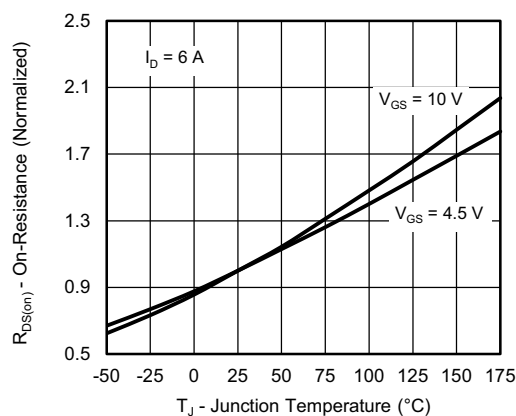
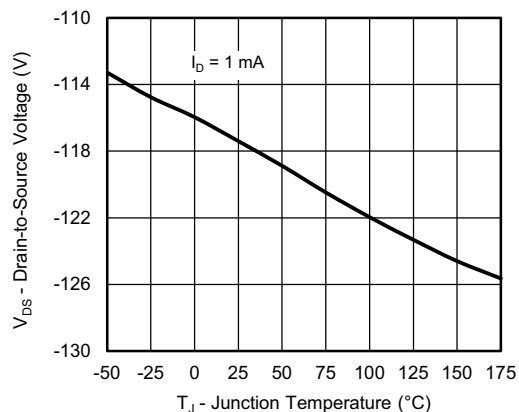
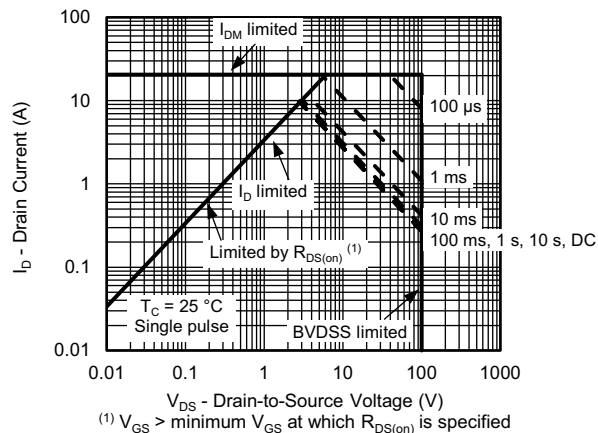
N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

On-Resistance vs. Junction Temperature

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area

N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case
Note

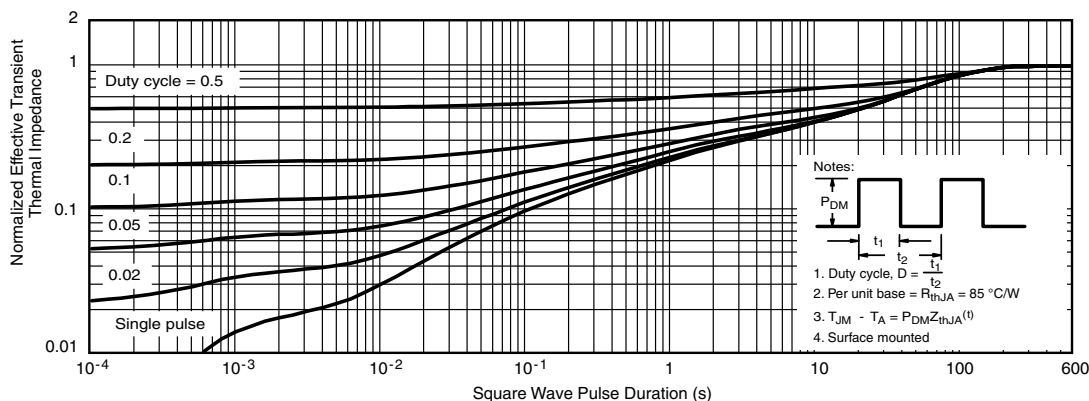
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

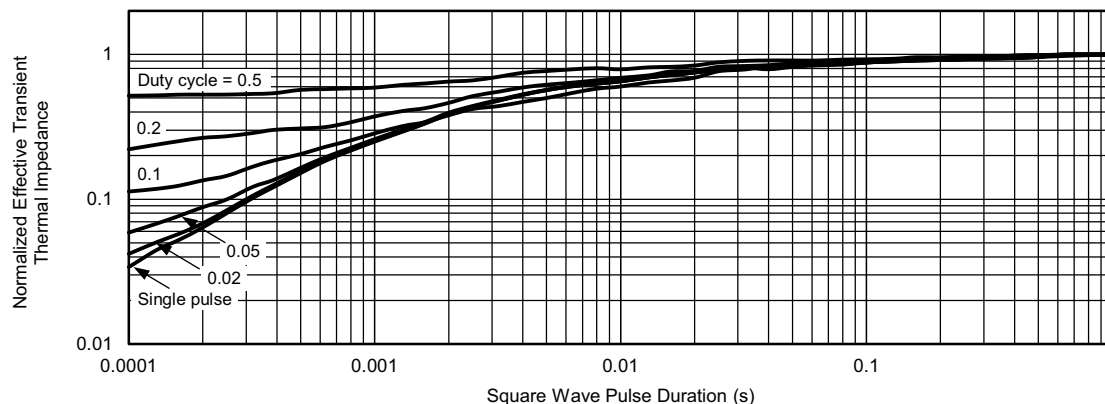
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Threshold Voltage

Source Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

On-Resistance vs. Junction Temperature

Drain Source Breakdown vs. Junction Temperature

Safe Operating Area



P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

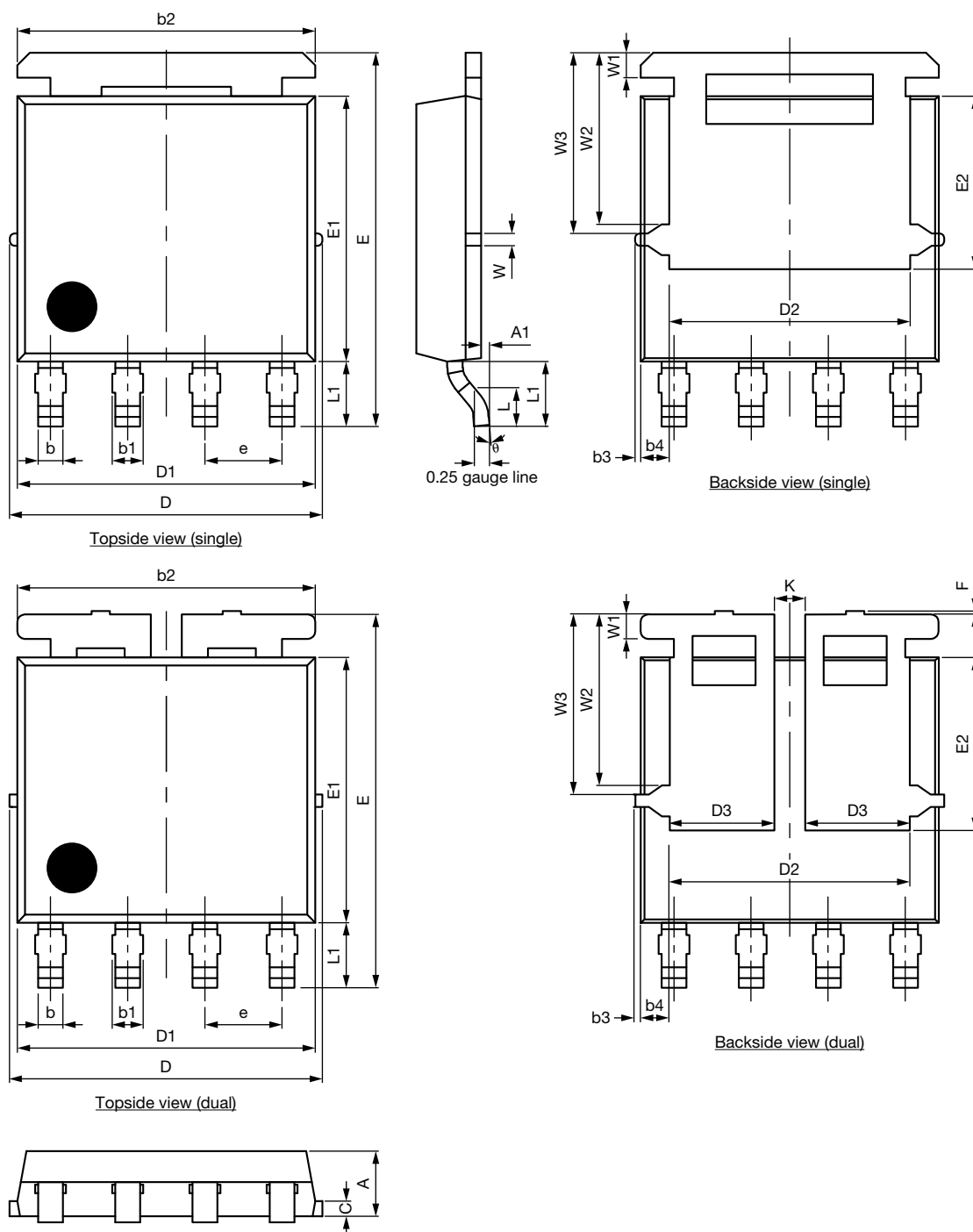
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^{\circ}\text{C}$)
 - Normalized Transient Thermal Impedance Junction-to-Case ($25\text{ }^{\circ}\text{C}$)
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76453.



PowerPAK® SO-8L Case Outline 2





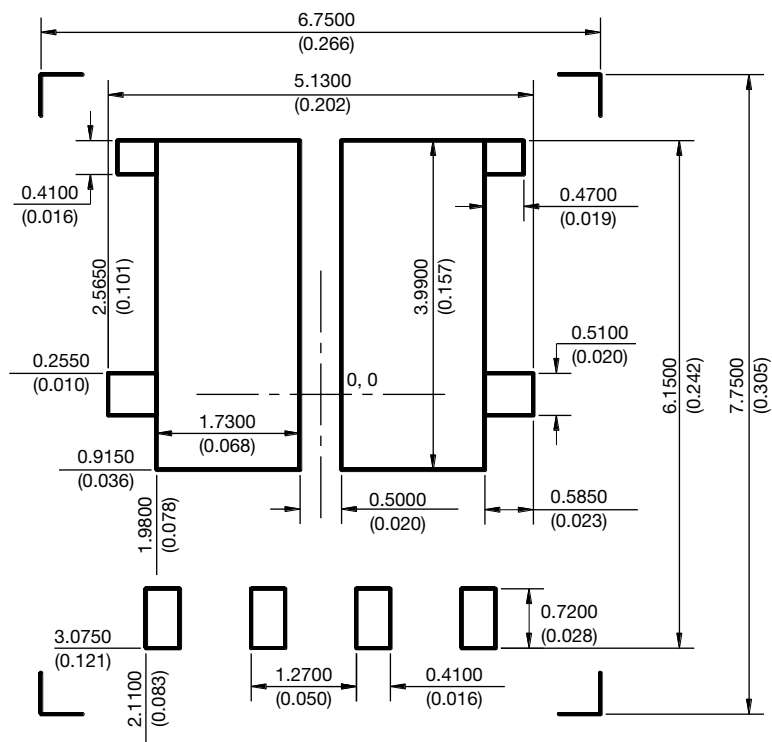
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	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.094			0.004		
b4	0.47			0.019		
c	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
e	1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.51			0.020		
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
θ	0°	-	10°	0°	-	10°
ECN: C21-1498-Rev. C, 01-Nov-2021						
DWG: 6044						

Note

- Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads
Dimensions in mm (inches)
Keep-out 6.75 (0.266) x 7.75 (0.305)



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