Single Thyristor (MAGN-A-PAK Block Power Module), 500 A

MAGN-A-PAK Block

FEATURES

- Electrically isolated base plate
- 3000 V_{RMS} isolating voltage
- Industrial standard package
- Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

APPLICATIONS

- Battery chargers
- Welders
- Power converters
- Alternators

PRIMARY CHARACTERISTICS	
$I_{T(AV)}$	500 A
Type	Modules - thyristor, standard
Package	MAGN-A-PAK block

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
V_{DRM}/V_{RRM}		800	V
$I_{T(AV)}$	76 °C	500	A
$I_{T(RMS)}$		785	
I_{TSM}	50 Hz	14 000	
	60 Hz	14 658	
I^2t	50 Hz	980	kA^2s
	60 Hz	894	
$I^2\sqrt{t}$		9800	$kA^2\sqrt{s}$
T_J	Range	-40 to +130	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS			
TYPE NUMBER	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 130 °C mA
VS-VSKS500/08PbF	800	900	80

ON-STATE CONDUCTION						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**VALUES**	**UNITS**
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction half sine wave			500	A
					76	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch			785	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sine half wave, initial $T_J = T_J$ maximum	16 646	
		t = 8.3 ms			17 430	
		t = 10 ms	100 % V_{RRM} reapplied		14 000	
		t = 8.3 ms			14 658	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		1385	kA^2s
		t = 8.3 ms			1265	
		t = 10 ms	100 % V_{RRM} reapplied		894	
		t = 8.3 ms			894	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			1385	$kA^2\sqrt{s}$
Low level value of threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J maximum			0.6839	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$), T_J maximum			0.7598	
Low level value on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J maximum			0.393	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$), T_J maximum			0.389	
Maximum on-state voltage drop	V_{TM}	T_J = 25 °C, I_{pk} = 500 A			1.1	V

SWITCHING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Typical delay time	t_d	Gate current 1 A, dI_g/dt = 1 A/µs, V_d = 0.67 % V_{DRM}, T_J = 25 °C, I_t = 400 A	1.3	µs
Typical turn-off time	t_q	I_{TM} = 750 A, $T_J = T_J$ maximum, dI/dt = 60 A/µs, V_R = 50 V, dV/dt = 20 V/µs, Gate 0 V 100 Ω, t_p = 500 µs	200	

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum linear to 67 % rated V_{DRM}	500	V/µs
Maximum peak reverse and off-state leakage current	I_{DRM}, I_{RRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	80	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminal shorted, t = 1 s	3000	V

TRIGGERING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10.0	W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50	2.0	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	3.0	A
Maximum required DC gate voltage to trigger	V_{GT}	T_J = 25 °C Anode supply: 12 V resistive load	3	V
Maximum required DC gate current to trigger	I_{GT}		200	mA
Maximum holding current	I_H		600	
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms	20	V
Maximum peak negative gate voltage	$-V_{GM}$		5.0	
DC gate voltage not to trigger	V_{GD}	$T_J = T_J$ maximum Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	0.30	V
DC gate current not to trigger	I_{GD}		10	mA
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ µs $T_J = T_J$ maximum, anode voltage ≤ 80 % V_{DRM}, I_t = 400 A	1000	A/µs

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNITS**
Maximum junction operating and storage temperature range	T_J, T_{Stg}		-40 to +130	°C
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.08	K/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface smooth, flat and greased	0.035	
Mounting torque ± 10 % MAGN-A-PAK block to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the spread of the compound. Lubricated threads.	6 to 8	Nm
Mounting torque ± 10 % busbar to MAGN-A-PAK block			12 to 15	
Approximate weight			430	g
			15.3	oz.
Case style			MAGN-A-PAK block	

ΔR CONDUCTION PER JUNCTION											
DEVICES	**SINUSOIDAL CONDUCTION AT T_J MAXIMUM**					**RECTANGULAR CONDUCTION AT T_J MAXIMUM**					**UNITS**
	180°	**120°**	**90°**	**60°**	**30°**	**180°**	**120°**	**90°**	**60°**	**30°**	
VS-VSKS500	0.013	0.0148	0.018	0.026	0.044	0.082	0.0142	0.019	0.027	0.044	K/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

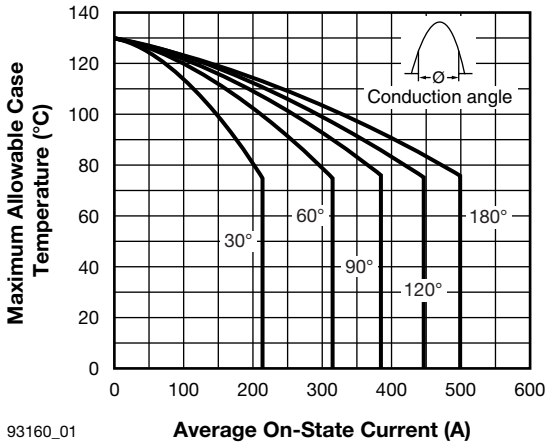


Fig. 1 - Current Rating Characteristics

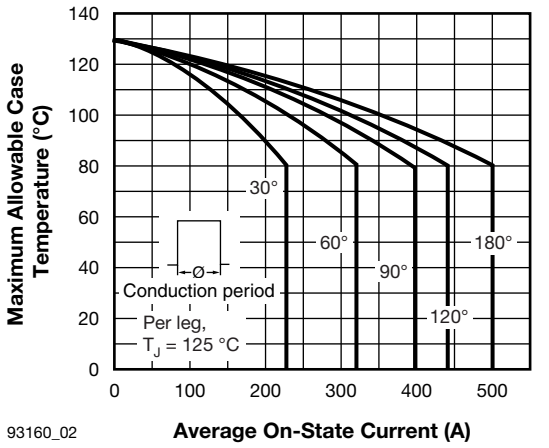


Fig. 2 - Current Rating Characteristics

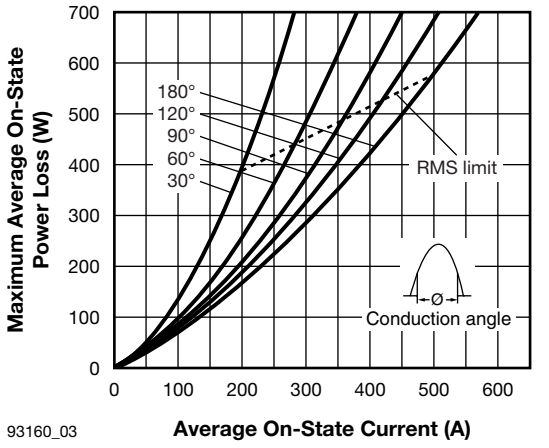


Fig. 3 - On-State Power Loss Characteristics

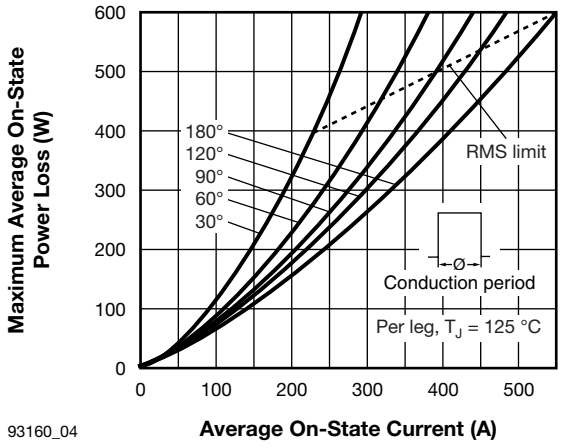


Fig. 4 - On-State Power Loss Characteristics

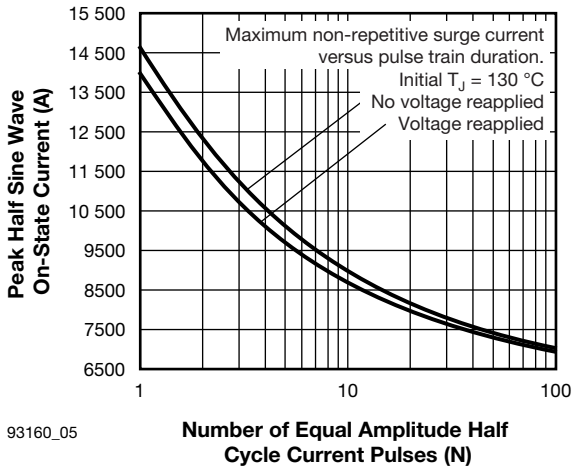


Fig. 5 - Maximum Non-Repetitive Surge Current

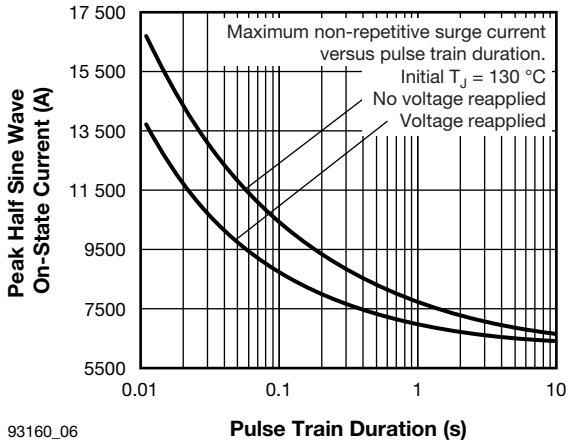


Fig. 6 - Maximum Non-Repetitive Surge Current

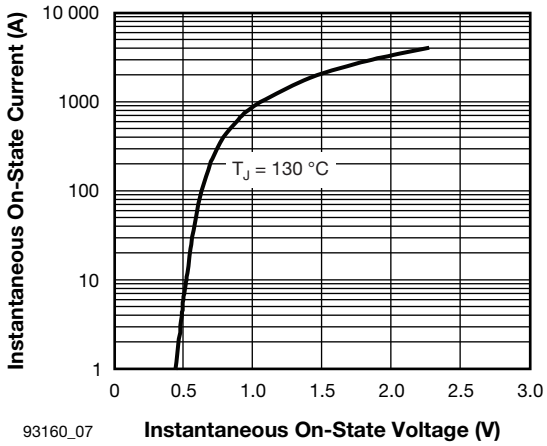


Fig. 7 - On-State Voltage Drop Characteristics

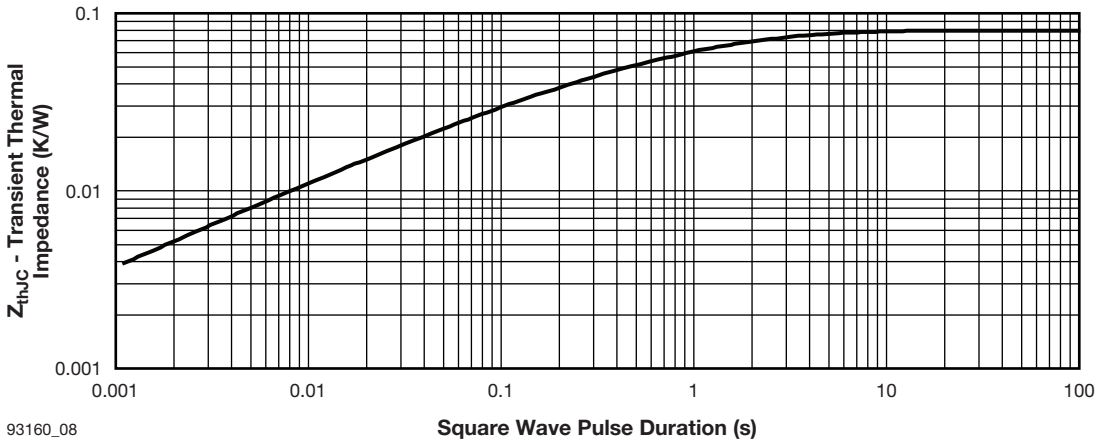


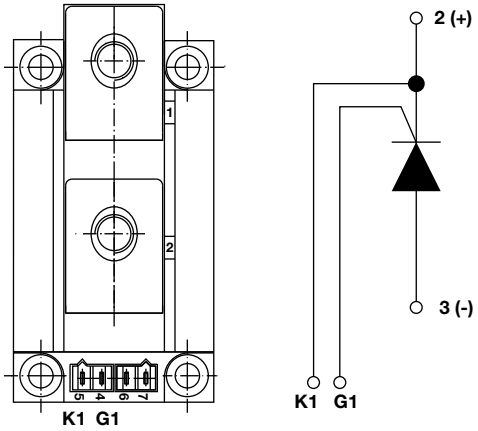
Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

ORDERING INFORMATION TABLE

Device code

VS-	VSK	S	500	/	08	PbF
1	2	3	4		5	6

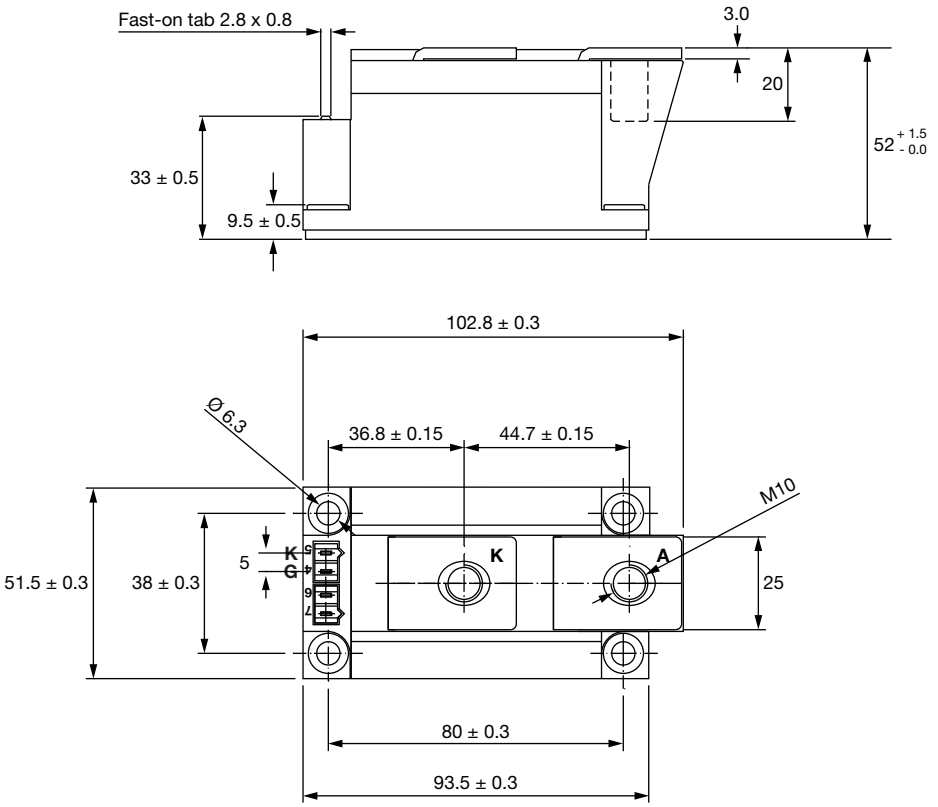
- 1 - Vishay Semiconductors product
- 2 - Module type
- 3 - Circuit configuration (S = single SCR)
- 4 - Current rating (500 = 500 A)
- 5 - Voltage rating (08 = 800 V)
- 6 - PbF = lead (Pb)-free

CIRCUIT CONFIGURATION	
CIRCUIT DESCRIPTION	**CIRCUIT DRAWING**
Single SCR	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95379

Thyristor MAP Block

DIMENSIONS in millimeters



Notes

- Dimensions are nominal
- Full engineering drawings are available on request

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.