User's Guide
SNVU676–June 2019

TLV803EA29EVM 3-Pin Voltage Supervisor User Guide

This user's guide describes the TLV803EA29EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

The TLV803EA29EVM is an evaluation module (EVM) for the TLV803E voltage supervisor also called a Reset IC. The TLV803EA29EVM can be used with any TLV803E, TLV809E, TLV803, and TLV809 devices variants, but please note that if using a push-pull device variant (TLV809E or TLV809), the shunt on J1 must be removed as push-pull devices do not use a pull-up resistor so R1 must be disconnected. The TLV803E has a supply voltage range of 1.7 V to 6 V, and offers connections for all device input and output pins. Test points are provided to give the user access to extra connections if needed for oscilloscope or multimeter measurements.

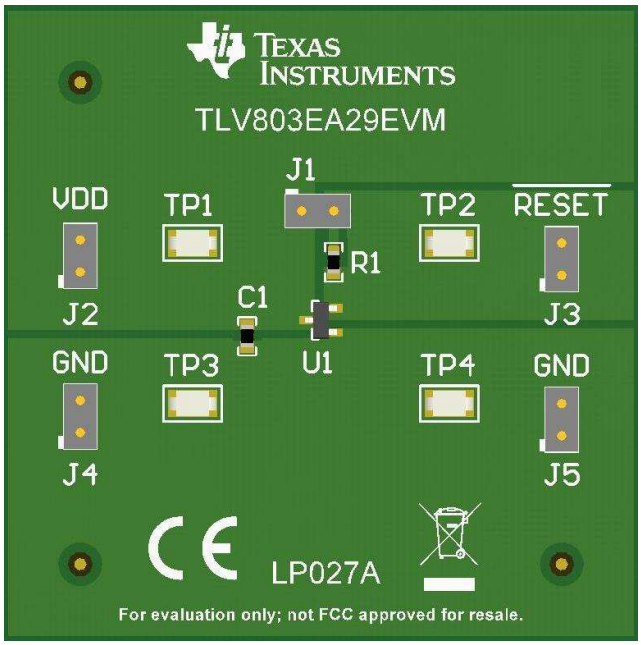

Figure 1. TLV803EA29EVM Board Top

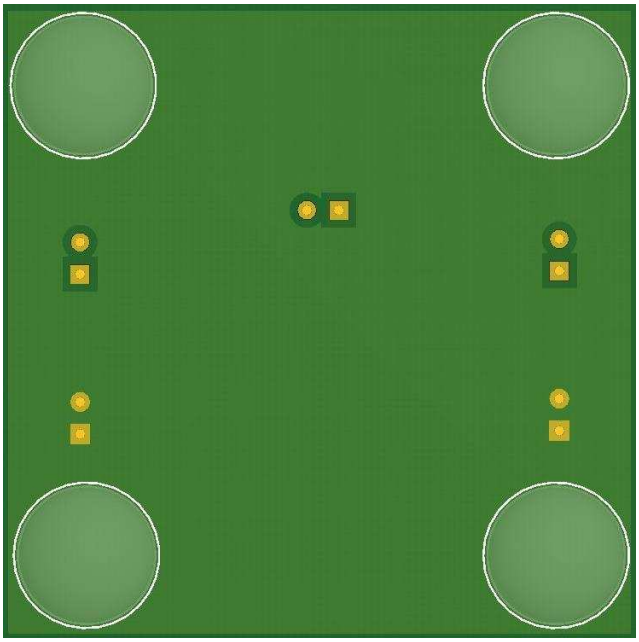

Figure 2. TLV803EA29EVM Board Bottom

1.1 Related Documentation

TLV803E / TLV809E Datasheet

1.2 TLV803E Applications

- Applications using DSPs, microcontrollers, or microprocessors
- Wireless communication systems
- Portable/battery-powered equipment
- Setup boxes and TVs
- Building automation
- Notebook/desktop computers, servers

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TLV803EA29EVM schematic, bill of materials (BOM), and layout.

2.1 TLV803EA29EVM Schematic

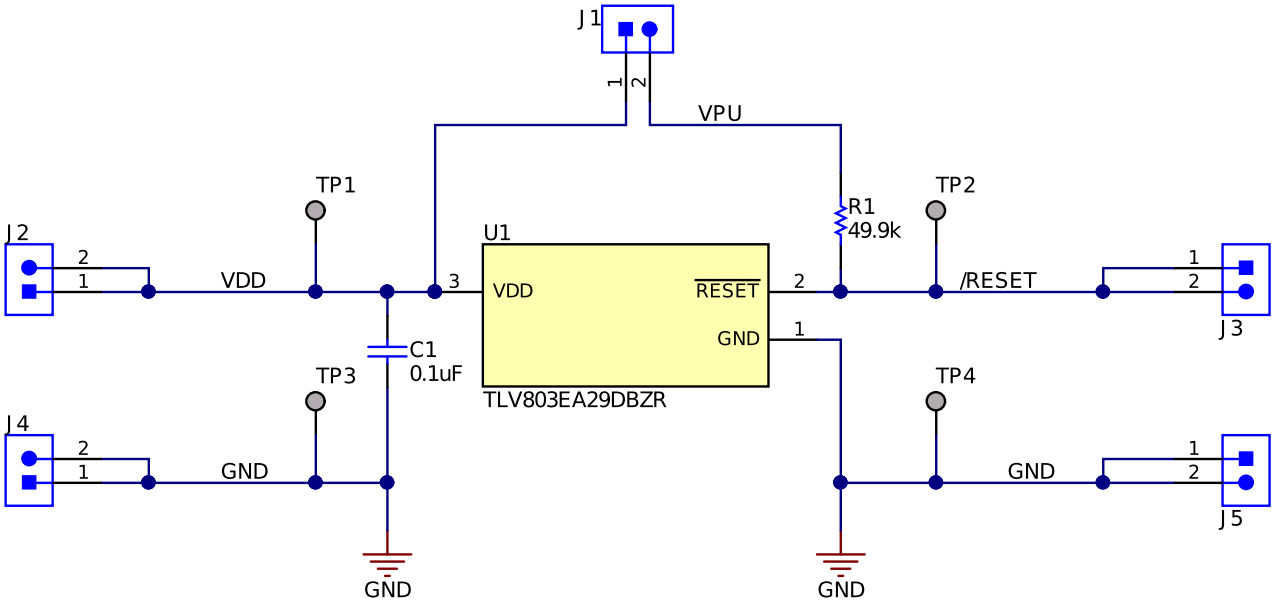

Figure 3. TLV803EA29EVM Schematic

2.2 TLV803EA29EVM Bill of Materials

Table 1. EVM BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		LP027	Any
C1	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	0603	C0603C104K8RACTU	Kemet
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J4, J5	5		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	800-10-002-10-001000	Mill-Max
R1	1	49.9k	RES, 49.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	ERJ-3EKF4992V	Panasonic
SH-J1	1		Shunt, 100mil, Tin plated, Black	Shunt Connector Black Open Top, 2x1	SNT-100-BK-T-H	Samtec
TP1, TP2, TP3, TP4	4		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		3-Pin Voltage Supervisors with Active-Low, Open-Drain Reset, DBZ0003A (SOT-23-3)	DBZ0003A	TLV803EA29DBZR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A

2.3 Layout and Component Placement

Figure 4 and Figure 5 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 6 and Figure 7 show the top and bottom layouts, Figure 8 and Figure 9 show the top and bottom layers, and Figure 10 shows the top solder mask of the EVM.

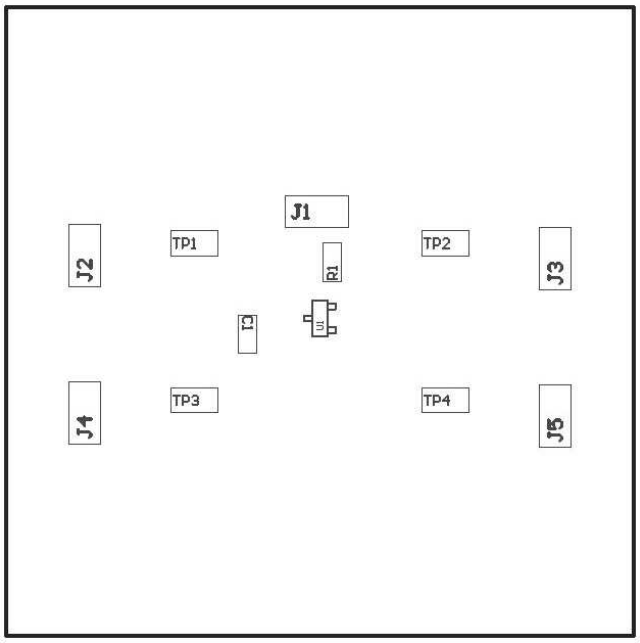

Figure 4. Component Placement—Top Assembly

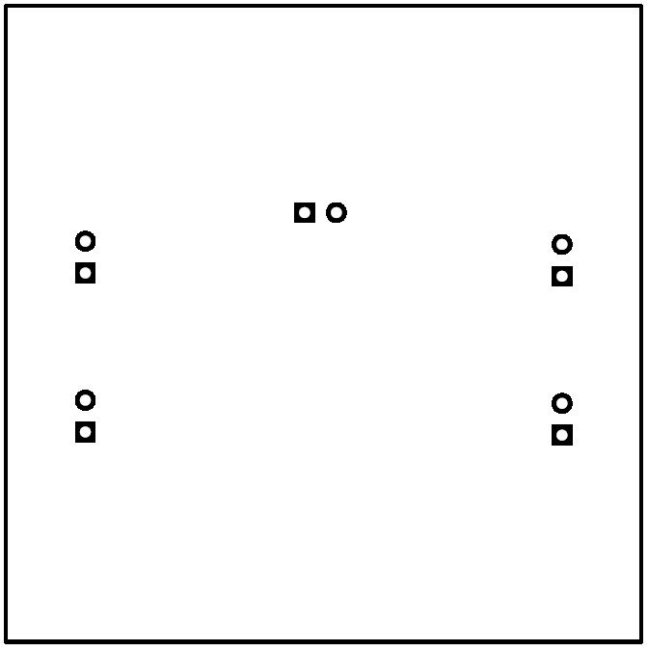

Figure 5. Component Placement—Bottom Assembly

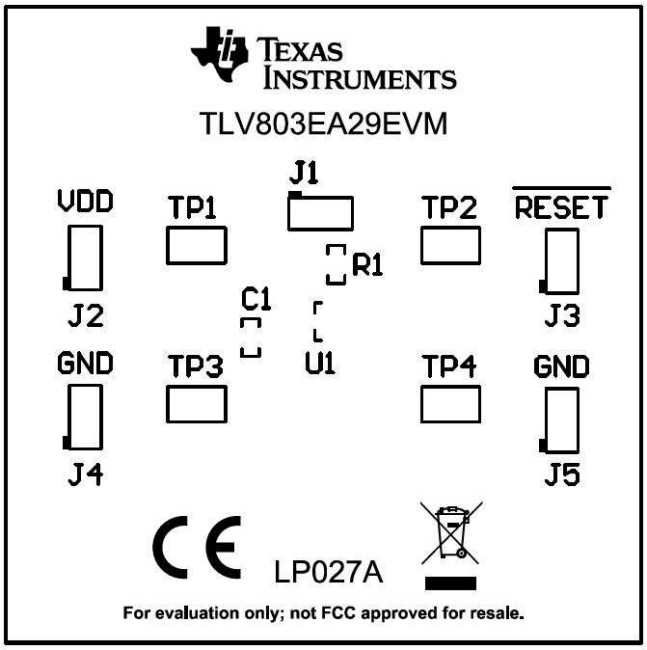

Figure 6. Layout—Top

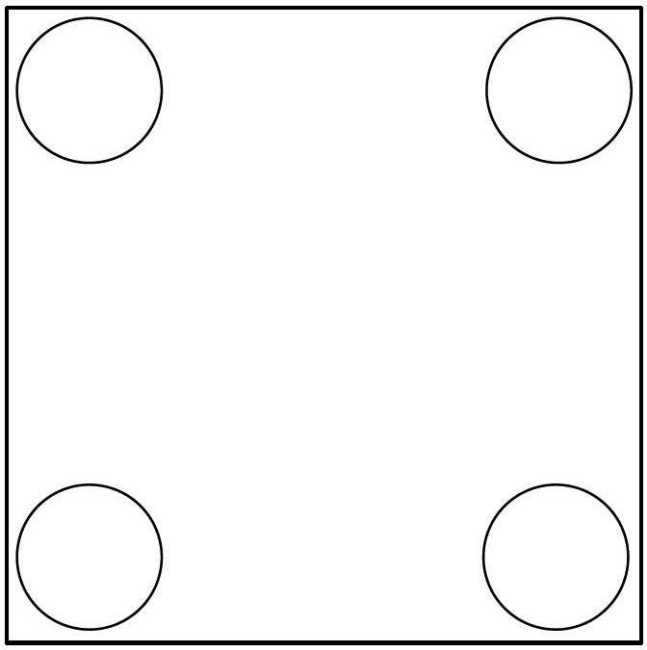

Figure 7. Layout—Bottom

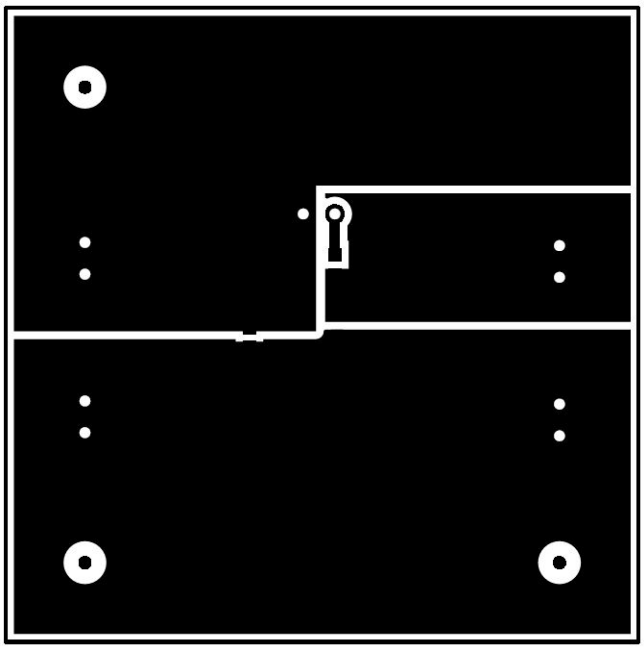

Figure 8. Top Layer

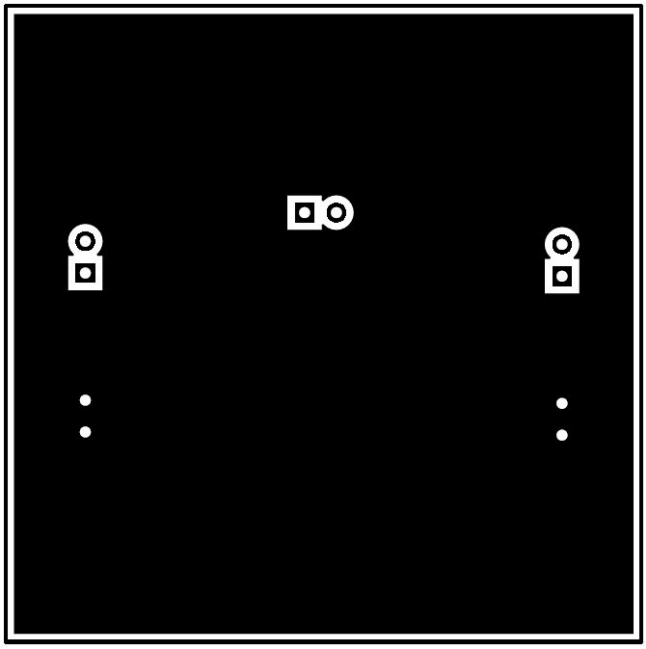

Figure 9. Bottom Layer

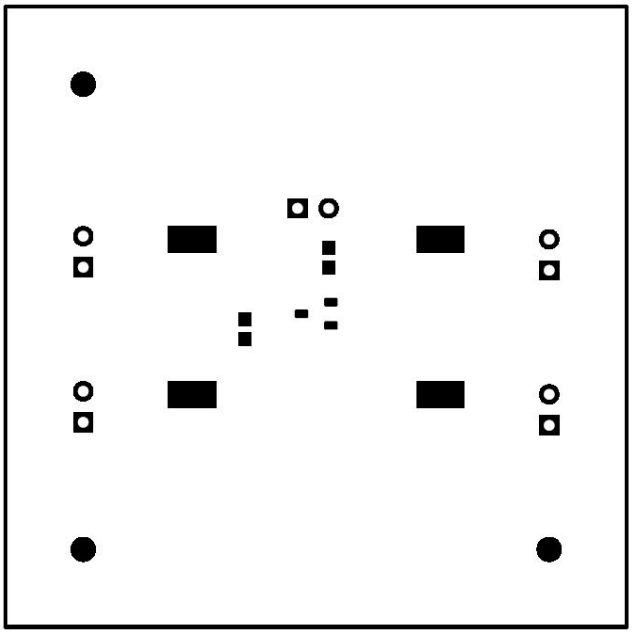

Figure 10. Top Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each EVM has an input power supply connection, and output $\overline{\text{RESET}}$ pin, and a ground pin.

3.1 EVM Test Points

Table 2 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 2. Test Points

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	VDD	Connection to VDD pin	Allows user to monitor the VDD pin. The VDD pin connects to the input power supply.
TP2	$\overline{\text{RESET}}$	Connection to $\overline{\text{RESET}}$ pin	Allows user to monitor the $\overline{\text{RESET}}$ pin. This pin changes logic state depending on the voltage on VDD.
TP3	GND	Connection to GND pin	Allows user to connect to the GND pin.
TP4	GND	Connection to GND pin	Allows user to connect to the GND pin.

3.2 EVM Jumpers

Table 3 lists the jumpers on the TLV803EA29EVM. As ordered, the EVM will have 5 jumpers populated.

Table 3. List of Onboard Jumpers

JUMPER	DEFAULT CONNECTION	DESCRIPTION
J1	Closed	Connect a shunt jumper to jumper J1 to use R1 as the pull-up resistor on the $\overline{\text{RESET}}$ output pin.
J2	Shorted	Both pins on J2 are connected together. Connect one of the pins to the positive (VDD) terminal of the power supply.
J3	Shorted	Both pins on J3 are connected together. Use either pin on jumper J3 to monitor the $\overline{\text{RESET}}$ output pin.
J4	Shorted	Both pins on J4 are connected together. Use either pin on jumper J4 as the ground connection.
J5	Shorted	Both pins on J5 are connected together. Use either pin on jumper J5 as the ground connection.

4 EVM Setup and Operation

This section describes the functionality and operation of the TLV803EA29EVM. The user must read the TLV803E / TLV809E Datasheet for electrical characteristics of the device.

4.1 Input Power (V_{DD})

The V_{DD} supply is connected through the J2 header on board. Both pins of jumper J2 are connected together so power can be applied to either pin. Supply voltage is dependent on what the user wants to monitor, but the range is 1.7 V to 6 V. Table 4 details the nominal supply and typical threshold voltage.

Table 4. Nominal Supply and Typical Threshold Voltages

DEVICE	NOMINAL SUPPLY VOLTAGE (V)	TYPICAL THRESHOLD VOLTAGE (V)
TLV803EA29	3.3	2.9 (+/- 2% MAX)

4.2 Monitoring Voltage on VDD

The TLV803E device monitors voltage via the VDD pin. The EVM provides jumper J2 and test point TP1 for connecting the power supply input to the VDD pin. If the voltage on this pin drops below V_{IT}, $\overline{RESET}$ is asserted low. The VDD pin is connected internally to a comparator through an internal resistor divider at the positive input and the negative input is connected to an internal reference. The internal resistor divider is set to provide the input voltage threshold to cause a reset, V_{IT-}, that corresponds to the chosen device variant. Please see the Device Comparison Table in the *TLV803E / TLV809E Datasheet* for more information on the different device variants.

Upon startup, the TLV803E requires VDD to be above V_{POR} before the $\overline{RESET}$ output is in the correct logic state. Figure 11 shows the propagation time delay high-to-low (t_{PDHL}) when a voltage fault occurs by VDD falling below V_{IT-} to the time $\overline{RESET}$ transitions active low. Figure 12 shows the reset time delay when the fault condition is removed by VDD rising above V_{IT+} to the time $\overline{RESET}$ transitions inactive high. The TLV803E has built-in glitch immunity so falling voltage transients on VDD are ignored if the falling pulse duration is less than the glitch immunity timing (t_{GI}). The glitch immunity specification depends on the amplitude of the voltage transient and the operating conditions. Please see the Glitch Immunity specification in the Timing Requirements section of the TLV803E / TLV809E Datasheet for more detailed information.

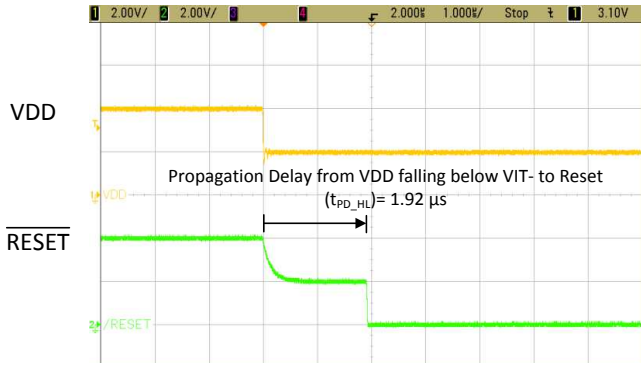

Figure 11. TLV803EA29EVM Propagation Delay Time High-to-Low (t_{PDHL})

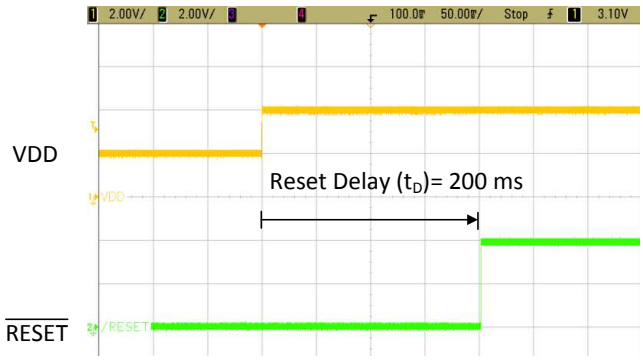

Figure 12. TLV803EA29EVM Reset Delay Time (t_D)

4.3 Reset Output ($\overline{RESET}$)

The TLV803EA29EVM comes populated with TLV803EA29 device variant which has open-drain, active-low output topology for the $\overline{RESET}$ pin. The other device variants provide different output topolgies and/or different voltage threshold options and can be used on this EVM. Note: if using a TLV809E device variant with push-pull output topology, the pull-up resistor must be disconnected by leaving jumper J1 open. The EVM provides a jumper J3 and a test point TP2 connected directly to the $\overline{RESET}$ pin for monitoring and/or interfacing to other devices. The reset signal will be asserted low when the voltage on the VDD pin falls below V_{IT-}. When the voltage on VDD rises higher than the hysteresis voltage above the threshold voltage (V_{HYS} + V_{IT-} or also labeled V_{IT+}), the $\overline{RESET}$ pin is pulled high to the inactive state indicating no fault condition. As Figure 13 shows, when returning from a fault condition, that is when VDD rises above V_{IT+}, VDD must be above V_{IT+} for longer than the reset delay (t_D) otherwise $\overline{RESET}$ will not transition back to logic high inactive state. This is to prevent a premature signaling of no fault condition if VDD briefly comes out of undervoltage condition before faulting again.

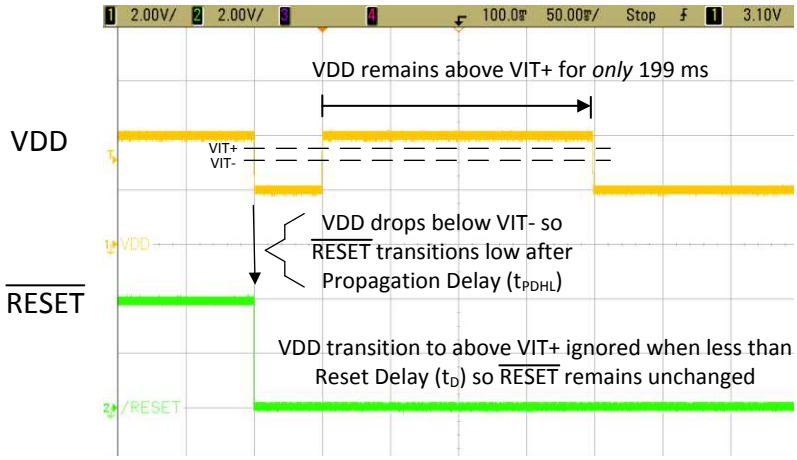

Figure 13. TLV803EA29EVM Return From Fault Glitch Immunity

Revision History

DATE	REVISION	NOTES
June 2019	*	Initial Release

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