FemtoClocks™ Crystal-TO-LVDS Frequency Synthesizer

844003-01

DATA SHEET

General Description

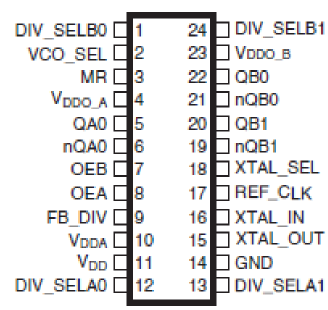
The 844003-01 is a 3 differential output LVDS Synthesizer designed to generate Ethernet refer- ence clock frequencies. Using a 19.53125MHz or 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (DIV_SELA[1:0], DIV_SELB[1:0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz. The 844003-01 has 2 output banks, Bank A with 1 differential LVDS output pair and Bank B with 2 differential LVDS output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 844003-01 uses IDT's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 844003-01 is packaged in a small 24-pin TSSOP package.

Features

- Three differential LVDS output pairs on two banks, Bank A with one LVDS pair and Bank B with two LVDS output pairs
- Using a 19.53125MHz or 25MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz - 680MHz
- RMS phase jitter @ 156.25MHz (1.875MHz – 20MHz): 0.56ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



844003-01

24-Lead TSSOP, E-Pad
4.40mm x 7.8mm x 0.925mm package body
G Package
Top View

Block Diagram

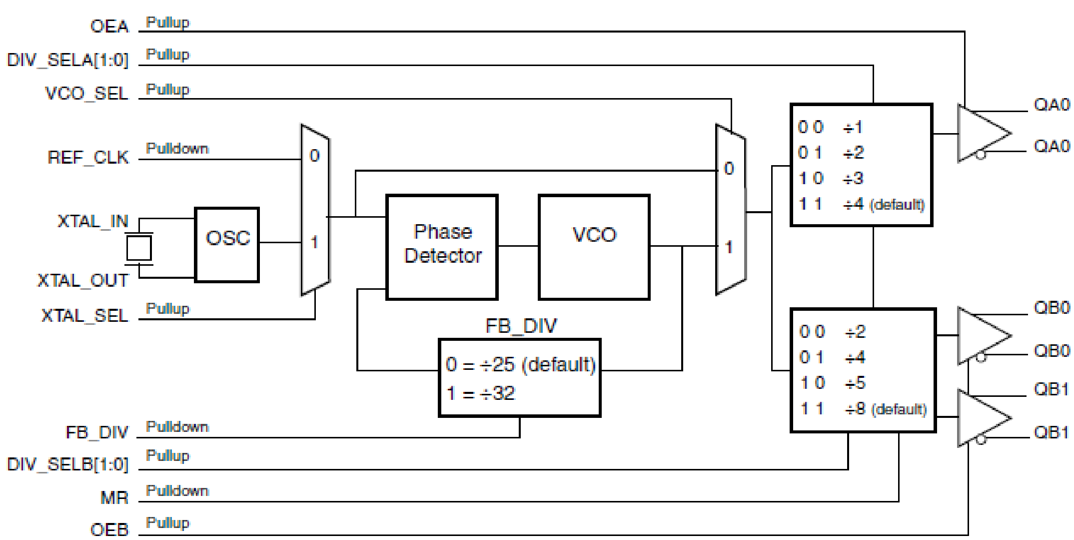


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 24	DIV_SELB0, DIV_SELB1	Input	Pullup	Division select pin for Bank B. Default = HIGH. LVCMOS/LVTTL interface levels. See Table 3B.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or REF_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
7	OEB	Input	Pullup	Output enable Bank B. Active High outputs are enable. When logic HIGH, the output pairs on Bank B are enabled. When logic LOW, the output pairs are in a high impedance state. Has an internal pullup resistor so the default power-up state of outputs are enabled. LVCMOS/LVTTL interface levels. See Table 3E.
8	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the output pair in Bank A is enabled. When logic LOW, the output pair is in a high impedance state. Has an internal pullup resistor so the default power-up state of output is enabled. LVCMOS/LVTTL interface levels. See Table 3D.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷25. When HIGH, the feedback divider is set for ÷32. See Table 3C. LVCMOS/LVTTL interface levels.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12, 13	DIV_SELA0, DIV_SELA1	Input	Pullup	Division select pin for Bank A. Default = HIGH. See Table 3A. LVCMOS/LVTTL interface levels.
14	GND	Power		Power supply ground.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	REF_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended REF_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
21, 22	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
23	V_{DDO_B}	Power		Output supply pin for Bank B outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Bank A Configuration Select Function Table

Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA0/ nQA0
0	0	÷1
0	1	÷2
1	0	÷3
1	1	÷4 (default)

Table 3B. Output Bank B Configuration Select Function Table

Inputs		Outputs
DIV_SELB1	DIV_SELB0	QB[0:1]/ nQB[0:1]
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷8 (default)

Table 3C. Feedback Divider Configuration Select Function Table

Input	
FB_DIV	Feedback Divide
0	÷25 (default)
1	÷32

Table 3D. OEA Select Function Table

Input	Outputs
OEA	QA0/ nQA0
0	High Impedance
1	Active (default)

Table 3E. OEB Select Function Table

Input	Outputs
OEB	QB[0:1]/ nQB[0:1]
0	High Impedance
1	Active (default)

Table 3F. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/ nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELA1	DIV_SELA0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.5	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

Table 3G. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QBx/ nQBx Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELB1	DIV_SELB0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	32.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				135	mA
I_{DDA}	Analog Supply Current				12	mA
$I_{DDO\_A} + I_{DDO\_B}$	Output Supply Current				80	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, MR, FB_DIV	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		DIV_SELA[0:1], OEA, OEB, DIV_SELB[0:1], VCO_SEL, XTAL_SEL	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, FB_DIV	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		DIV_SELA[0:1], OEA, OEB, DIV_SELB[0:1], VCO_SEL, XTAL_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		250		450	mV

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25	1.33	1.41	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷25		19.6		27.2	MHz
	FB_DIV = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

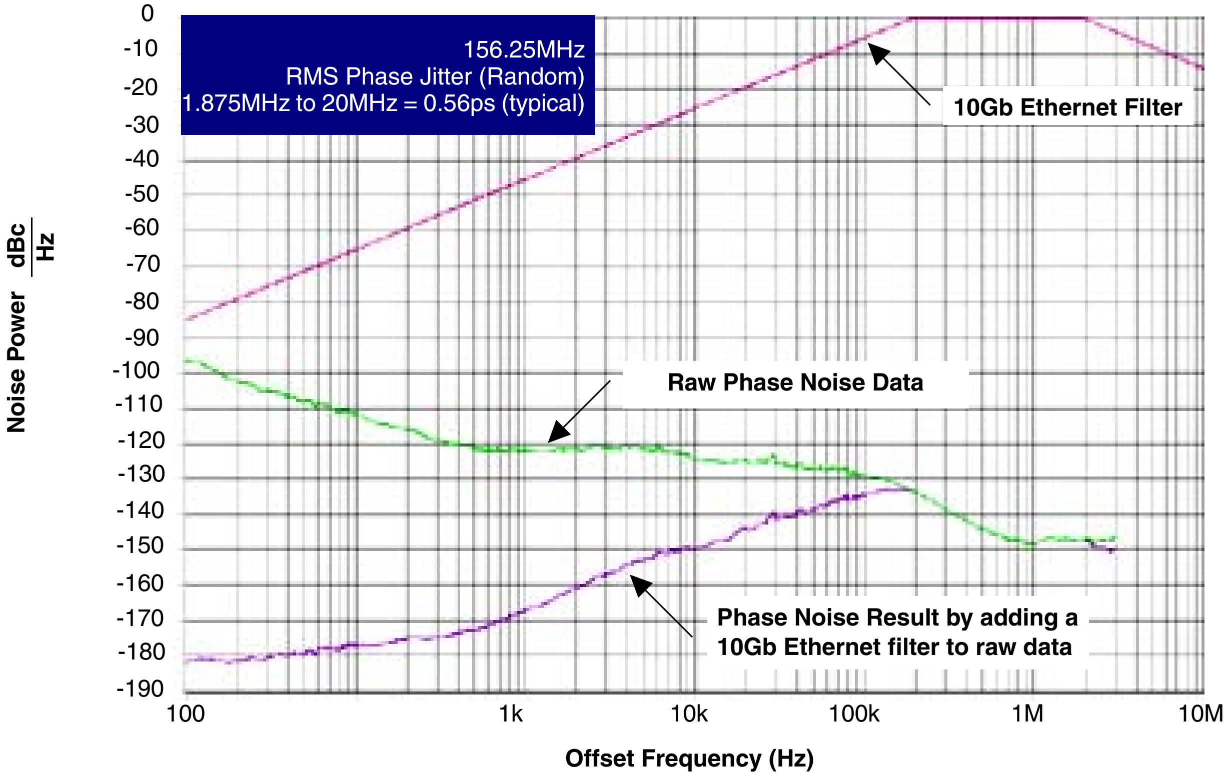
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

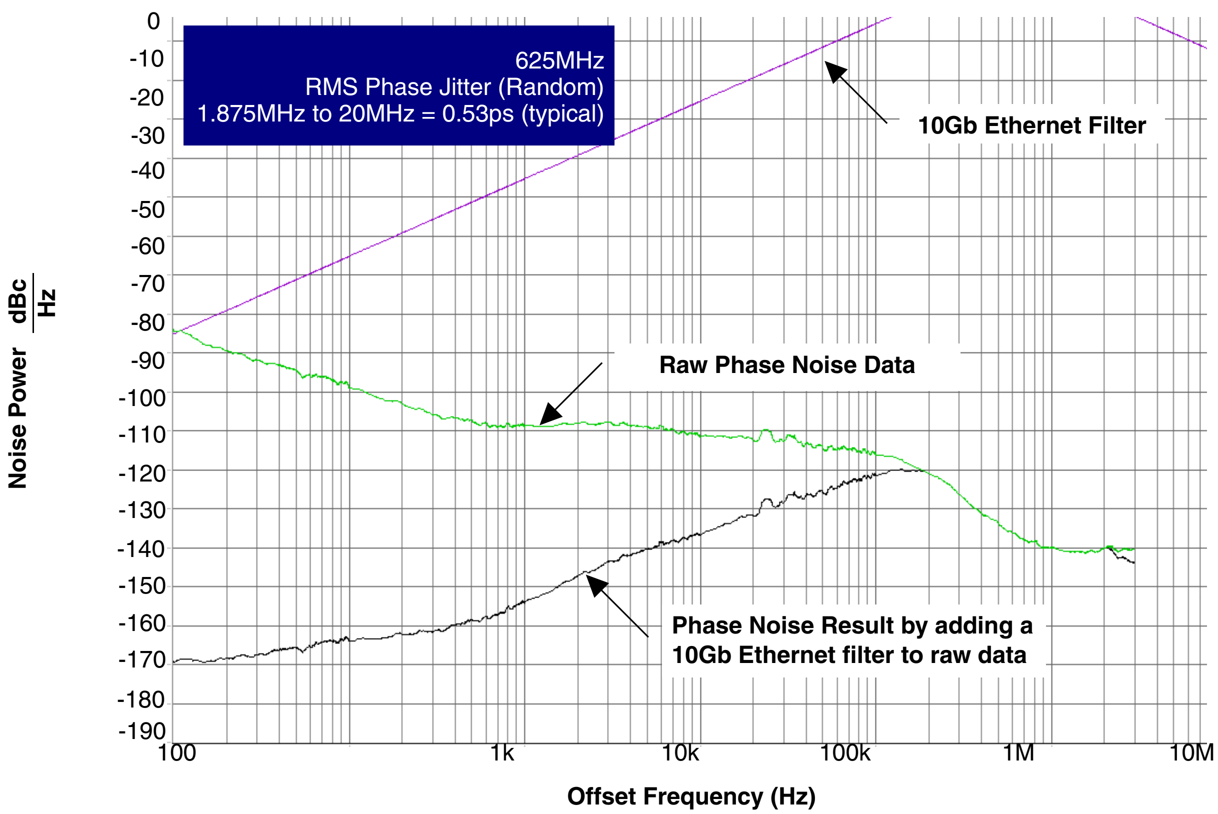
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range		Output Divider = ÷1	490		680	MHz
			Output Divider = ÷2	245		340	MHz
			Output Divider = ÷3	163.33		226.67	MHz
			Output Divider = ÷4	122.5		170	MHz
			Output Divider = ÷5	98		136	MHz
			Output Divider = ÷8	61.25		85	MHz
*t*sk(b)	Bank Skew; NOTE 1					33	ps
*t*sk(o)	Output Skew	NOTE 2, 3	Outputs @ Same Frequency			75	ps
		NOTE 2, 3, 4	Outputs @ Different Frequencies			170	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 5		625MHz (1.875MHz – 20MHz)		0.53		ps
			312.5MHz (1.875MHz – 20MHz):		0.53		ps
			156.25MHz (1.875MHz – 20MHz)		0.56		ps
			125MHz (1.875MHz – 20MHz)		0.58		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	200		450	ps
odc	Output Duty Cycle		Output Divider ≠ ÷1	47		53	%
			Output Divider = ÷1	43		57	%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Characterized using output dividers 1, 2, 4, 8.
NOTE 5: Refer to the Phase Noise Plots.

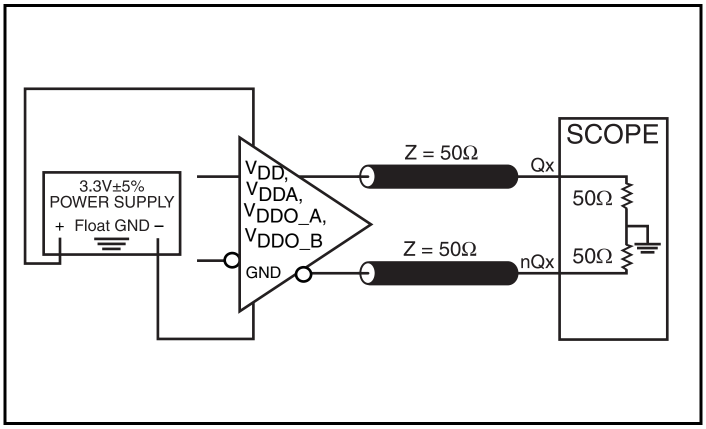
Typical Phase Noise at 156.25MHz



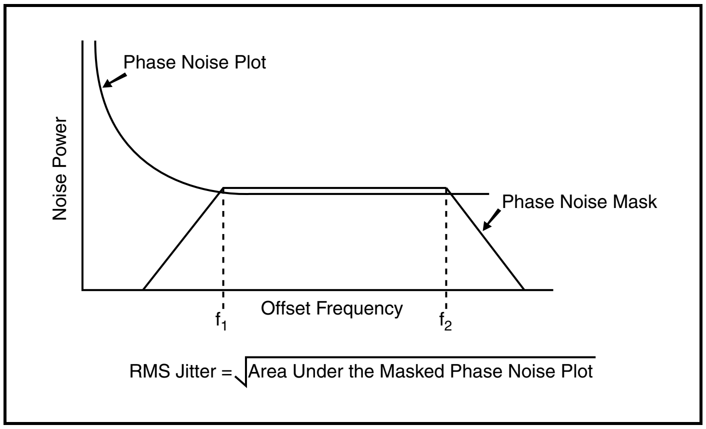
Typical Phase Noise at 625MHz



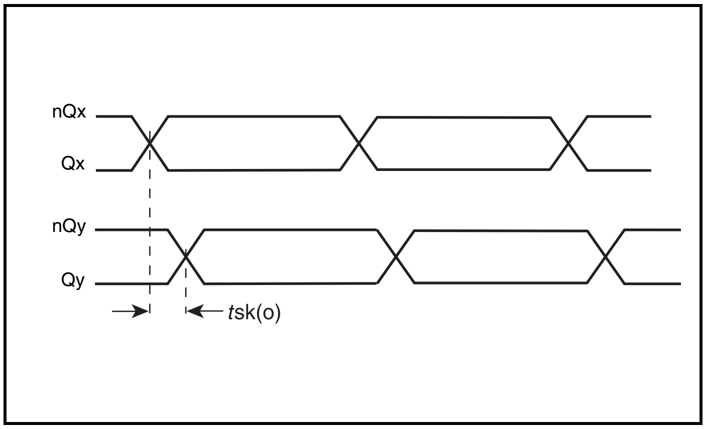
Parameter Measurement Information



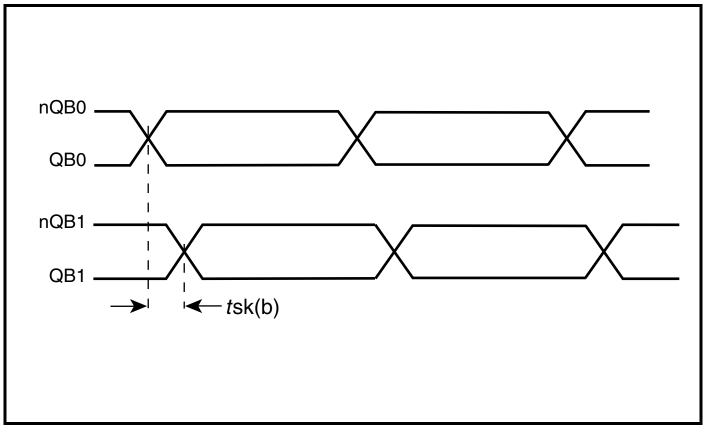
3.3V LVDS Output Load AC Test Circuit



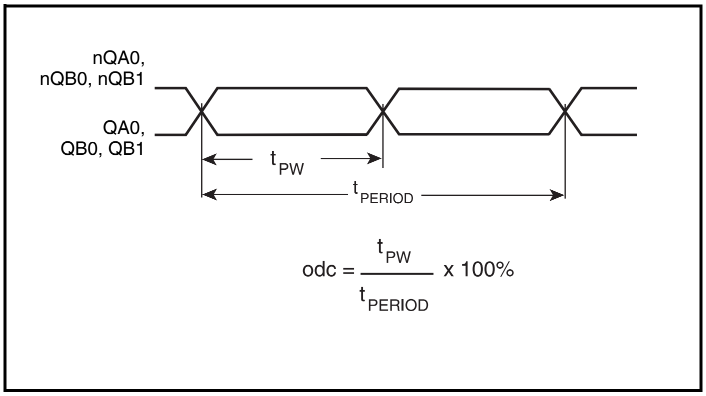
RMS Phase Jitter



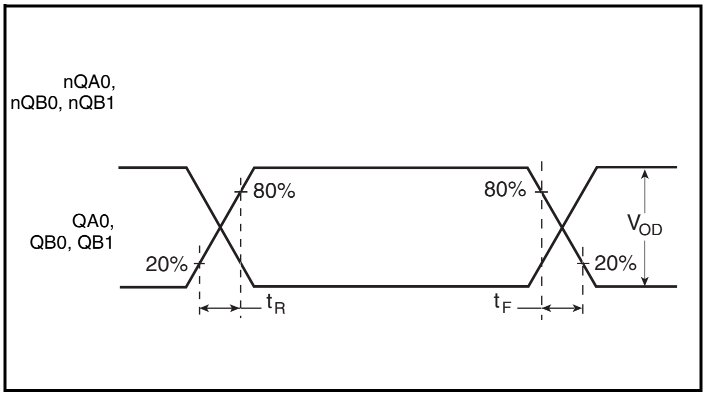
Output Skew



Bank Skew

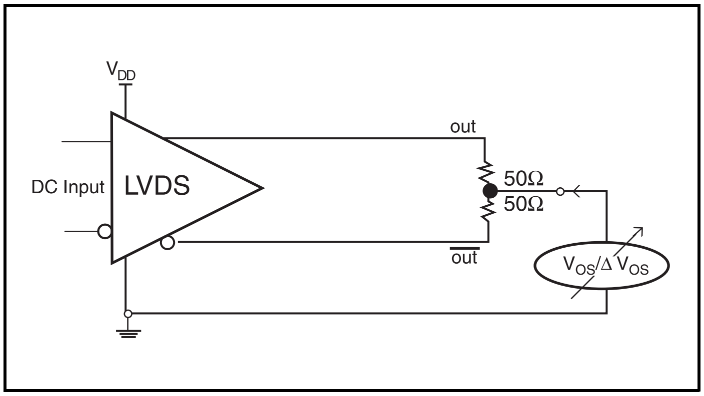


Output Duty Cycle/Pulse Width/Period

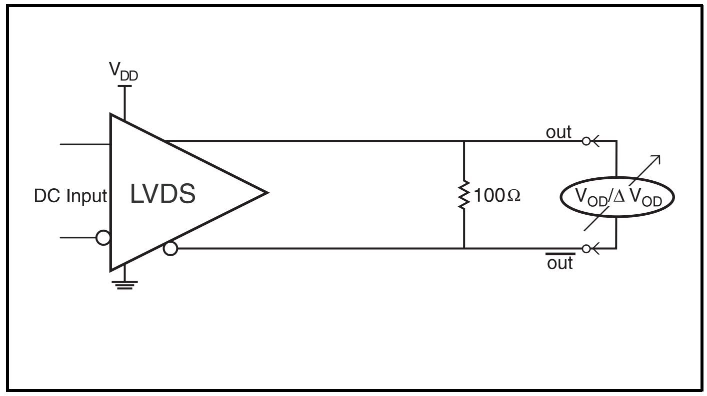


Output Rise/Fall Time

Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter perform- ance, power supply isolation is required. The 844003-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO_A} and V_{DDO_B} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

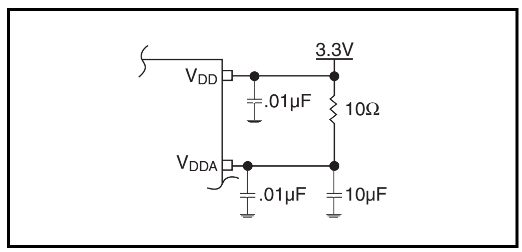


Figure 1. Power Supply Filtering

Crystal Input Interface

The 844003-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 19.53125MHz or 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

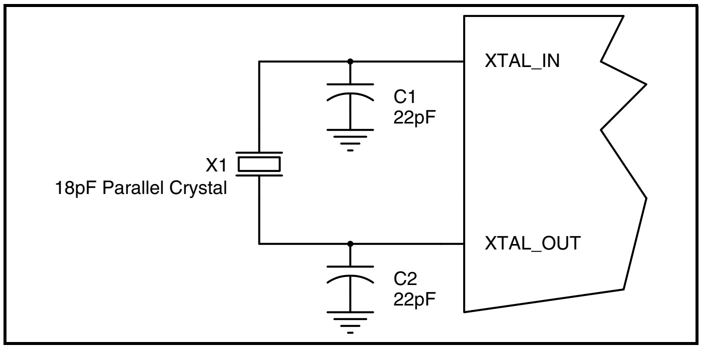


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

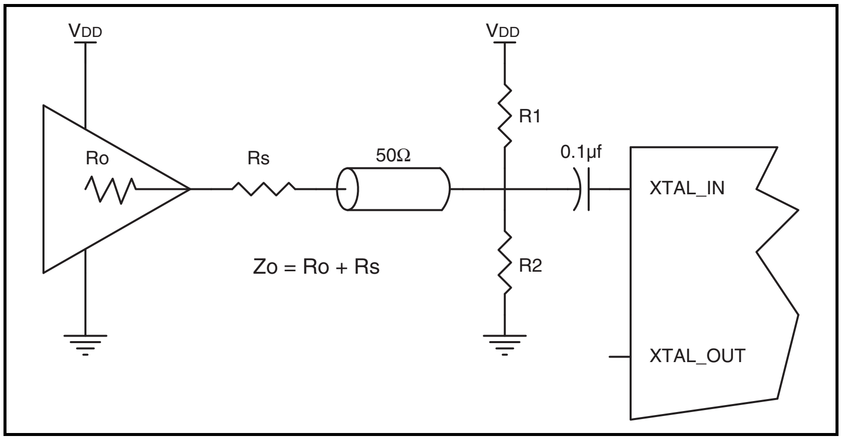


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 4* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

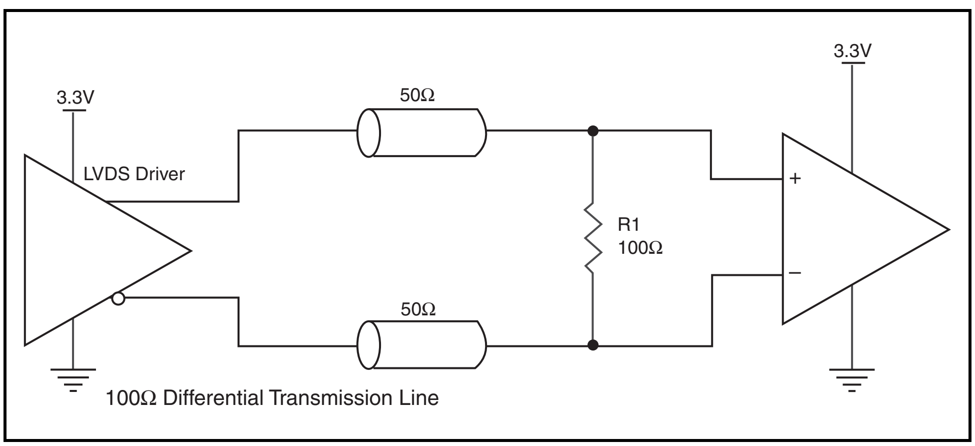


Figure 4. Typical LVDS Driver Termination

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

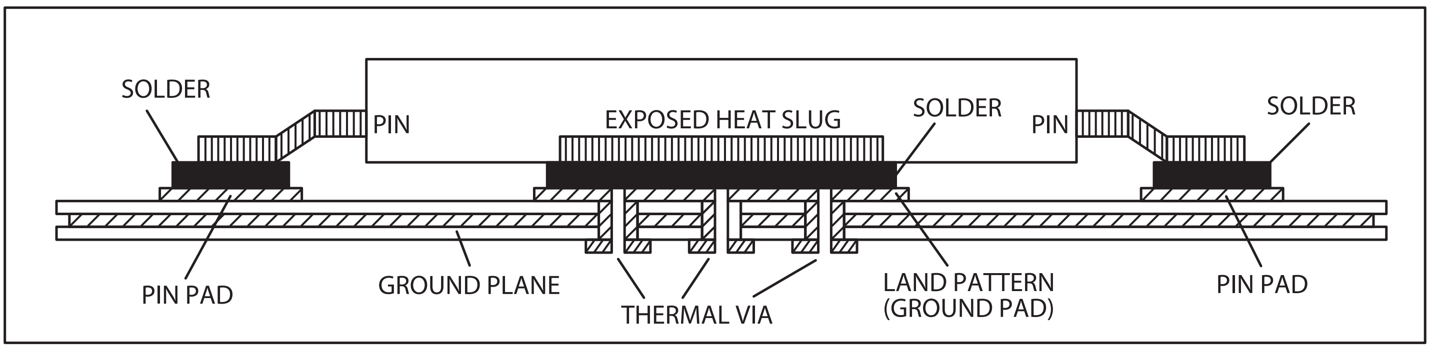


Figure 5. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 844003-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844003-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (135mA + 12mA) = **509.36mW**
- Power $(outputs)_{MAX} = V_{DDO\_MAX} * I_{DDO\_MAX}$ = 3.465V * 80mA = **277.20mW**

Total Power$_{\_MAX}$ = 509.36mW + 277.20mW = **786.56mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.787W * 32.1°C/W = 95.3°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board.

Table 7. Thermal Resistance θ_{JA} for 24 Lead TSSOP, E-Pad, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	35.5°C/W	26.9°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP, E-Pad

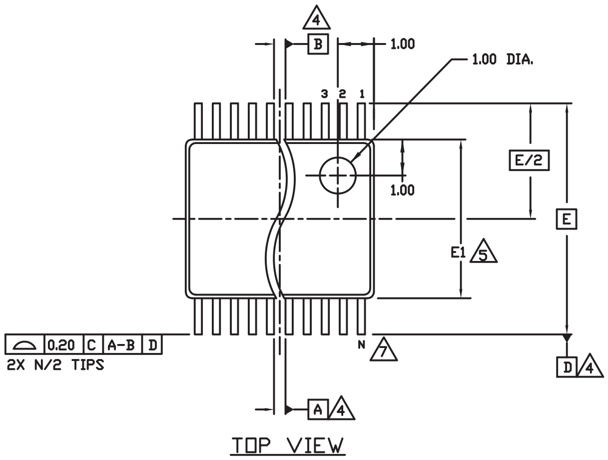
θ_{JA} **by Velocity**			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	32.1°C/W	35.5°C/W	26.9°C/W

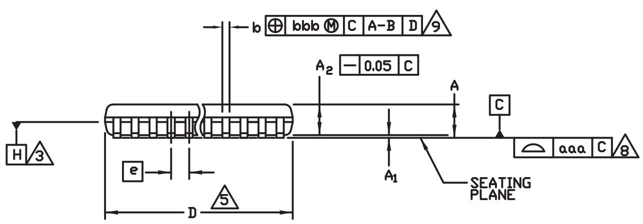
Transistor Count

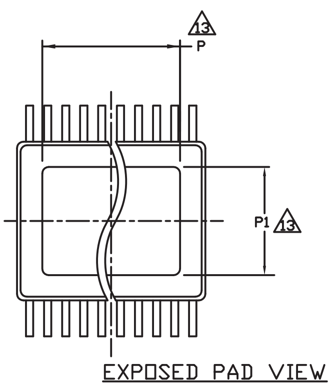
The transistor count for 844003-01 is: 3537

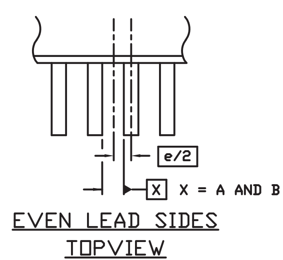
Package Outline and Package Dimensions

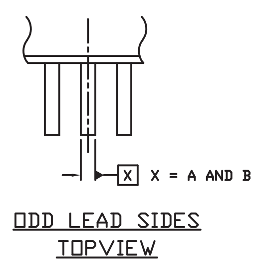
Package Outline - G Suffix for 24 Lead TSSOP, E-Pad

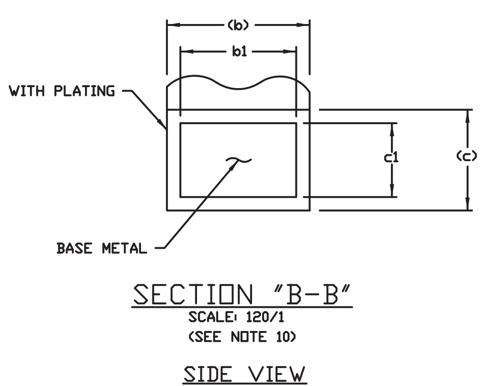


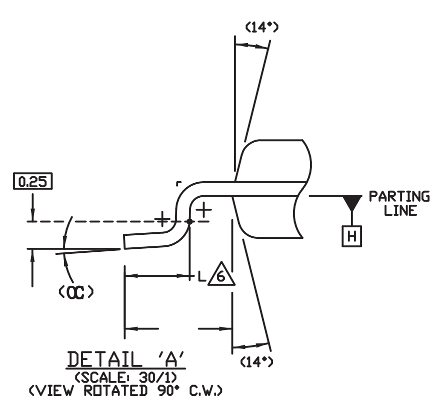












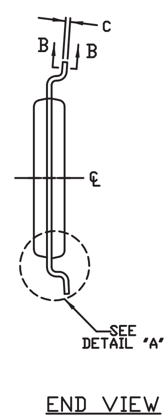


Table 9. Package Dimensions

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		24	
A			1.10
A1	0.05		0.15
A2	0.85	0.90	0.95
b	0.19		0.30
b1	0.19	0.22	0.25
c	0.09		0.20
c1	0.09	0.127	0.16
D	7.70		7.90
E		6.40 Basic	
E1	4.30	4.40	4.50
e		0.65 Basic	
L	0.50	0.60	0.70
P	5.0		5.5
P1	3.0		3.2
α	0°		8°
ααα		0.076	
bbb		0.10	

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844003BG-01LF	ICS844003B01L	“Lead-Free” 24 Lead TSSOP, E-Pad	Tube	0°C to 70°C
844003BG-01LFT	ICS844003B01L	“Lead-Free” 24 Lead TSSOP, E-Pad	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	1 18	Features section - removed bullet referencing leaded devices Ordering Information - removed leaded devices. Updated data sheet format.	6/10/15

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