SX1302

LoRa Gateway Baseband Processor

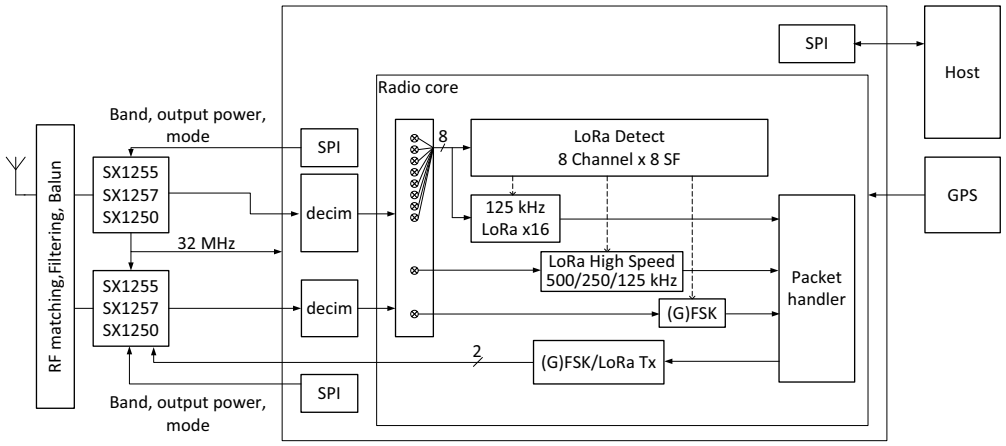


Figure A: Block Diagram

General Description

The SX1302 is a new generation of baseband LoRa® chip for gateways. It excels in reducing current consumption, simplifies the thermal design of gateways, and reduces the Bill Of Materials costs, yet it is capable of handling a higher amount of traffic than preceding devices.

The high-speed baseband digital engines are clocked from a single 32 MHz clock source, and the chip embeds the capability to support SF5 and SF6 unlike previous generations. To absorb the additional traffic that the radio will be able to detect, more modems are now collaborating. 8 of them have been added to specifically handle the high-speed SF5 and SF6 packets, whilst the 8 others are still taking care of the SF7-SF12 traffic. The architecture has been reworked to reduce power consumption very significantly; it makes it easier to embed the SX1302 in highly-integrated environments where power dissipation might be a challenge.

The SX1302 is also serialized in production, with a globally unique 64-bit number.

Key Features

- LoRaWAN, Class A/B/C, all regions
- 125 kHz LoRa reception with:
  - 8 x 8 channels LoRa® packet detectors
  - 8 x SF5-SF12 LoRa® demodulators
  - 8 x SF5-SF10 LoRa® demodulators
- 125 /250 / 500 kHz LoRa® demodulator
- (G)FSK demodulator
- Direct interface to Semtech transceivers
- SX1255, SX1257 and SX1250
- Single 32 MHz clock

Ordering Information

Part Number	Delivery	Order Quantity
SX1302IMLTRT	Tape and Reel	3000

QFN68 Package, operating range from -40 to +85°C

Pb-free, Halogen free, RoHS/WEEE compliant product

Revision History

Version	ECO	Date	Modifications
Rev 1.0	ECO-047283	June 2019	First Release
Rev 1.1	ECO-050134	January 2020	Add specification for the sequencing of VCC_CORE and VCC_IO in Section 5.
Rev 1.2	ECO-053763	October 2020	Update title to "LoRa Gateway Baseband Processor" Edit the link to the HAL/Packet Forwarder repository

Table of Contents

General Description 1
Key Features 1
Ordering Information 1
Revision History 2
List of Figures 5
List of Tables 6
1. Introduction 7
    1.1 RF Front End Interface 7
    1.2 Power Distribution 7
    1.3 Clocking 7
    1.4 Detection Engine and Modems 7
    1.5 Digital Interface and Control 7
    1.6 Application Programming Interface 7
    1.7 Application Information 7
2. Pin Connections 8
    2.1 Pinout 8
    2.2 Package View 11
3. Specifications 12
    3.1 ESD Notice 12
    3.2 Absolute Minimum and Maximum Ratings 13
    3.3 Operating Range 13
    3.4 Electrical Specifications 13
    3.5 Digital I/O Specifications 14
    3.6 Example Reference Design Performance 14
4. RF Front End Interface 16
5. Power Distribution 18
6. Clocking 19
7. Detection Engine - Modems 20
8. Digital Interface and Control 21
    8.1 Host SPI Interface 21
        8.1.1 HOST SPI Timings 21
        8.1.2 SPI Timings 22
9. Application Programming Interface 23
    9.1 Globally Unique EUI 23
10. Application Information 24
    10.1 Geographical Designs 24
    10.2 Reference Block Diagram 24
    10.3 Reference Design Layout 25
11. Packaging Information 26
    11.1 Package Outline Drawing 26
    11.2 Package Marking 27
    11.3 Land Pattern 27
    11.4 Reflow Profiles 28

11.5 Tape and Reel Specification 28
11.6 Thermal Impedance 28
Glossary 29

List of Figures

Figure 2-1: Pin Locations, Top View 11
Figure 4-1: Receive Interconnection 16
Figure 4-2: Transmit Interconnection 16
Figure 5-1: VCC_CORE and VCC_IO Sequencing 18
Figure 8-1: SPI Timing Diagram 21
Figure 10-1: Application Design Block Diagram 24
Figure 10-2: Reference Design PCB Layout 25
Figure 11-1: QFN 7x7 Package Outline Drawing 26
Figure 11-2: SX1302 Package Marking 27
Figure 11-3: QFN 7x7mm Land Pattern 27
Figure 11-4: Tape and Reel Specification 28

List of Tables

Table 2-1: Pinout 8
Table 3-1: ESD and Latch-Up Notice 12
Table 3-2: Minimum and Maximum Ratings 13
Table 3-3: Operating Range 13
Table 3-4: Performances 13
Table 3-5: Digital I/O Specifications 14
Table 3-6: Reference Design Performance 14
Table 4-1: Semtech RF Front-end Summary 17
Table 5-1: Current Consumption 18
Table 8-1: SPI Timing Requirements 22
Table 11-1: Tape and Reel Specification 28

1. Introduction

The SX1302 is a digital baseband engine, capable of detecting and demodulating large amounts of LoRa® packets expected in the IOT networks.

1.1 RF Front End Interface

The SX1302 is intended to be used with various RF Front End chips (RF to IQ), such as Semtech's SX1255/57. Details on the interface and compatibility is available on Section 4. "RF Front End Interface" on page 16 .

1.2 Power Distribution

The SX1302 is supplied on two different domains, 1.2 V for the core of the baseband processing, and 3 to 3.6V for the host and RF interface. For details, see Section 5. "Power Distribution" on page 18 .

1.3 Clocking

SX1302 clocking is achieved from a single clock source. Details are found in Section 6. "Clocking" on page 19 .

1.4 Detection Engine and Modems

The SX1302 can detect at any time, any packet in a combination of 8 different spreading factors (SF5 to SF12) and 10 channels, and demodulate up to 16 packets at any time. Details on the modems and their assignment are found in Section 7. "Detection Engine - Modems" on page 20 .

1.5 Digital Interface and Control

The SPI interface of the SX1302 to its host controller is detailed in Section 8. "Digital Interface and Control" on page 21 .

1.6 Application Programming Interface

An example API is made available as source code with the HAL library and the Packet Forwarder example software. Details are available in Section 9. "Application Programming Interface" on page 23 .

1.7 Application Information

Semtech has designed, validated, and released multiple reference design with the SX1302. The performance tabulated in this document is obtained on the said reference design. Details of the Core Cell reference design are posted in Section 10. "Application Information" on page 24 .

2. Pin Connections

2.1 Pinout

Table 2-1: Pinout

Pin Number	Pin Name	Direction	Description	SX1250	SX1255/57
(0)	GND	Power	Ground		
1	HOST_CSN	Input	External HOST SPI CSN pin		
2	HOST_MISO	Output	External HOST SPI MISO pin		
3	HOST_MOSI	Input	External HOST SPI MOSI pin		
4	HOST_SCK	Input	External HOST SPI SCK pin		
5	VCC_CORE	Power	Core supply		
6	GND	Power	Ground		
7	RESET	Input	Asynchronous Reset Input		
8	PPS	Input	PPS input from GPS		
9	GND	Power	Ground		
10	RADIO_CTRL[0]	Output	Radio A Enable LDO		
11	RADIO_CTRL[1]	Output	Radio A Enable LNA and control switch		
12	RADIO_CTRL[2]	Output	Radio A Enable PA and control switch		
13	RADIO_CTRL[3]	Output	Radio A Reset	NRESET	RESET
14	VCC_IO	Power	IO supply		
15	GND	Power	Ground		
16	RADIO_CTRL[4]	Output	Radio A PA gain_0		
17	RADIO_CTRL[5]	Output	Radio A PA gain_1		
18	RADIO_B_CSN	Output	Radio B SPI CSN pin	NSS	NSS
19	RADIO_B_MOSI	Output	Radio B SPI MOSI pin	MOSI	MOSI
20	SP_VALID	Input	Stream synchronization for FPGA		
21	RADIO_B_SCK	Output	Radio B SPI SCK pin	SCK	SCK
22	RADIO_CTRL[6]	Output	Radio B Enable LDO		
23	VCC_CORE	Power	Core supply		

Table 2-1: Pinout

Pin Number	Pin Name	Direction	Description	SX1250	SX1255/57
24	GND	Power	Ground		
25	GND	Power	Ground		
26	RADIO_CTRL[7]	Output	Radio B Enable LNA and control switch		
27	RADIO_CTRL[8]	Output	Radio B Enable PA and control switch		
28	RADIO_CTRL[9]	Output	Radio B Reset	NRESET	RESET
29	RADIO_CTRL[10]	Output	Radio B PA gain_0		
30	VCC_IO	Power	IO supply		
31	RADIO_CTRL[11]	Output	Radio B PA gain_1		
32	RADIO_B_IQ[3]	I/O - NS		DIO4	I_OUT
33	RADIO_B_MISO	Input		MISO	MISO
34	RADIO_B_CLK_I	Input		BUSY	CLK_OUT
35	RADIO_B_IQ[0]	I/O - NS		DIO1	Q_OUT
36	RADIO_B_IQ[1]	I/O - NS		DIO2	I_IN
37	RADIO_B_IQ[4]	I/O - NS		DIO5	Q_IN
38	RADIO_B_IQ[2]	I/O - NS		DIO3	CLK_IN
39	GND	Power	Ground		
40	VCC_CORE	Power	Core supply		
41	RADIO_A_IQ[3]	I/O - NS		DIO4	I_OUT
42	RADIO_A_MISO	Input		MISO	MISO
43	RADIO_A_CLK_I	Input		BUSY	CLK_OUT
44	RADIO_A_IQ[0]	I/O - NS		DIO1	Q_OUT
45	RADIO_A_IQ[1]	I/O - NS		DIO2	I_IN
46	GND	Power	Ground		
47	VCC_IO	Power	IO supply		
48	RADIO_A_IQ[4]	I/O - NS		DIO5	Q_IN
49	RADIO_A_IQ[2]	I/O - NS		DIO3	CLK_IN
50	GPIO[11]	In/out	General purpose IO		
51	GPIO[10]	In/out	General purpose IO		

Table 2-1: Pinout

Pin Number	Pin Name	Direction	Description	SX1250	SX1255/57
52	GPIO[9]	In/out	General purpose IO		
53	GPIO[8]	In/out	General purpose IO		
54	GPIO[7]	In/out	General purpose IO		
55	GND	Power	Ground		
56	VCC_CORE	Power	Core supply		
57	GPIO[6]	In/out	General purpose IO		
58	GPIO[5]	In/out	General purpose IO		
59	GPIO[4]	In/out	General purpose IO		
60	GPIO[3]	In/out	General purpose IO		
61	VCC_IO	Power	IO supply		
62	GND	Power	Ground		
63	GPIO[2]	In/out	General purpose IO		
64	GPIO[1]	In/out	General purpose IO		
65	RADIO_A_SCK	Output	Radio A SPI SCK pin	SCK	SCK
66	GPIO[0]	Input	General purpose IO		
67	RADIO_A_MOSI	Output	Radio A SPI MOSI pin	MOSI	MOSI
68	RADIO_A_CSN	Output	Radio A SPI CSN pin	NSS	NSS
(0)	GND	Power	Ground		

2.2 Package View

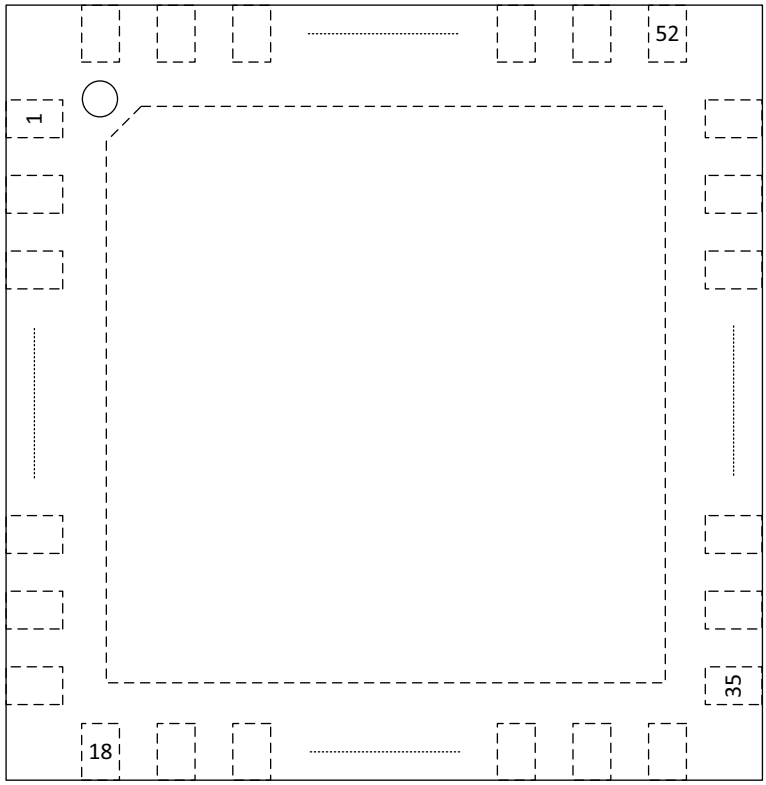


Figure 2-1: Pin Locations, Top View

3. Specifications

All measured performances and conditions are listed in this chapter. Quantitative indications left in other chapters are for the ease of reading and are indicative only.

The following specifications are given for the typical operating conditions of VCC_IO = VBAT = 3.3 V, temperature = 25 °C (85°C for maximum values), reference oscillator frequency = 32 MHz, RF centre frequency = 868 MHz. All RF impedances are matched using the reference design, see Section 10.2 "Reference Block Diagram" on page 24. Blocking, ACR and co-channel rejection are given for a single tone interferer and referenced to sensitivity level +6 dB.

3.1 ESD Notice

The SX1302 has built-in ESD and latch-up protection.

It should however be handled with all the necessary ESD precautions to avoid any permanent damage.

Table 3-1: ESD and Latch-Up Notice

Symbol	Description	Min	Typ	Max	Unit
ESD_HBM	Class 2 of ANSI/ESDA/JEDEC Standard JS-001-2014 (Human Body Model)	-	-	2	kV
ESD_CDM	ESD Charged Device Model, JEDEC standard JESD22-C101, class C4	-	-	500	V
LU	Latch-up, JEDEC standard JESD78 B, class I level A	-	-	100	mA

3.2 Absolute Minimum and Maximum Ratings

Table 3-2: Minimum and Maximum Ratings

Symbol	Description	Min	Max	Unit
$V_{CCIO,ABSMAX}$	IO power supply to VSS	-0.5	4.0	V
$V_{CCcore,ABSMAX}$	Core power supply to VSS	-0.5	1.5	V
T_{STORE}	Storage temperature	-40	+125	°C
T_{REFLOW}	Peak reflow temperature		260	°C
MSL	Humidity rating		MSL1	

3.3 Operating Range

Table 3-3: Operating Range

Symbol	Description	Minimum	Typical	Maximum	Unit
$V_{CCIO,OP}$	IO supply operating conditions	3.0	3.3	3.6	V
$V_{CCCORE,OP}$	Core supply operating conditions	1.1	1.2	1.3	V
$T_{A,OP}$	Operating temperature	-40	25	+85	°C

3.4 Electrical Specifications

Table 3-4, “Performances,” on page 13 summarizes the electrical performance of the SX1302, over operating conditions. The reference design described in Section 10. "Application Information" on page 24 is used to measure this performance.

Table 3-4: Performances

Symbol	Description	Min	Typ	Max	Unit
IDD_8CH_CORE	Average consumption when all correlators are active (no packet detected, no modem activated), on VCC_CORE	-	15	-	mA
IDD_8CH_IO	Average consumption when all correlators are active (no packet detected, no modem activated), on VCC_IO	-	1	-	mA
IDD_8CH_AVG_CORE	Average consumption when all correlators are active, and 16 modems are active, on VCC_CORE	-	17	77	mA
IDD_8CH_PEAK_CORE	Peak[1] consumption when all correlators are active, and 16 modems are active, on VCC_CORE	-	28	85	mA
IDD_8CH_AVG_IO	Average consumption when all correlators are active, and 16 modems are active, on VCC_IO	-	1	-	mA

Table 3-4: Performances

Symbol	Description	Min	Typ	Max	Unit
IDD_TX_CORE	Sending data on SX1250 using SF6, average, on VCC_CORE	-	7.2	-	mA
IDD_TX_IO	Sending data on SX1250 using SF6, average, on VCC_IO	-	1.4	-	mA
IDD_OFF_CORE	OFF current, clock is disabled, on VCC_CORE	-	3.2	-	mA
IDD_OFF_IO	On VCC_IO	-	10	-	uA
FERR	Frequency Offset Tolerance, less than 3dB degradation[2]	-	-	+/-0.25* BW	Hz

1. Average and Peak current concepts are explained in Section 5. on page 18
2. Capability to receive a LoRa® signal with frequency offset on the carrier, assuming a precision of up to +/-0.5ppm on the reference frequency of the SX1302-based design. For instance, for LoRa® Bandwidth of 125 kHz, incoming packets can be offset by up to +/-31 kHz.

3.5 Digital I/O Specifications

Table 3-5: Digital I/O Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
VIH	Input High Voltage	-	0.7*VCC_IO	-	VCC_IO + 0.3	V
VIL	Input Low Voltage		-0.3	-	0.3*VCC_IO	V
VOH	Output High Voltage	I_{max} = -8 mA	VCC_IO - 0.6	-	VCC_IO	V
VOL	Output Low Voltage	I_{max} = 8mA	0	-	0.4	V

All inputs are floating and should be driven to a proper potential to avoid current leakage in low-power modes. GPIO[i] pins have a selectable internal 100 kOhms pull-down resistor, when configured as inputs, and they are disabled at Reset.

3.6 Example Reference Design Performance

Disclaimer: the performance specifications listed below are only indicative, and obtained on the reference design described in Section 10.2 "Reference Block Diagram" on page 24.

Sensitivity is specified with a PER=10%, receiving 12 Byte packets, all under nominal temperature and voltage conditions. It is measured with a SX1250 front-end, an LNA with 18dB of gain and 1.5 dB of Noise Figure.

Table 3-6: Reference Design Performance

Symbol	Description	Min	Typ	Max	Unit
S_SF5_125	SF5 Sensitivity, LoRa 125 kHz bandwidth	-	-121	-	dBm
S_SF6_125	SF6 Sensitivity, LoRa 125 kHz bandwidth	-	-123.5	-	dBm
S_SF7_125	SF7 Sensitivity, LoRa 125 kHz bandwidth	-	-127	-	dBm
S_SF8_125	SF8 Sensitivity, LoRa 125 kHz bandwidth	-	-129	-	dBm

Table 3-6: Reference Design Performance

Symbol	Description	Min	Typ	Max	Unit
S_SF9_125	SF9 Sensitivity, LoRa 125 kHz bandwidth	-	-132.5	-	dBm
S_SF10_125	SF10 Sensitivity, LoRa 125 kHz bandwidth	-	-135.5	-	dBm
S_SF11_125	SF11 Sensitivity, LoRa 125 kHz bandwidth	-	-138	-	dBm
S_SF12_125	SF12 Sensitivity, LoRa 125 kHz bandwidth	-	-141	-	dBm
S_FSK_50	50 kbps, GFSK modulation	-	-111	-	dBm
S_SF9_250	SF9 Sensitivity, LoRa 250 kHz bandwidth	-	-126.5	-	dBm

A complete performance report of the reference design published in Section 10.2 "Reference Block Diagram" on page 24 is posted on www.semtech.com.

4. RF Front End Interface

The SX1302 can accommodate any of the following RF front-end devices: SX1250, SX1255 and SX1257, all of which are Semtech products. For any other device, hardware logic could be used on the interface for translation purposes.

The roles of these devices is to down-convert the RF signal to baseband (direct conversion or low-IF), and digitize it to feed the IQ samples to the SX1302 baseband chip.

The interconnection to the front-end device is organized as follows. Here, the SX1250 is taken as an example:

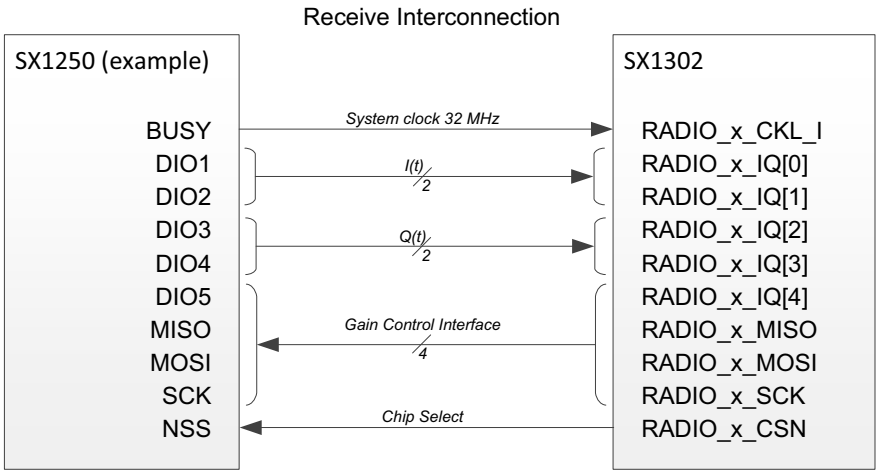


Figure 4-1: Receive Interconnection

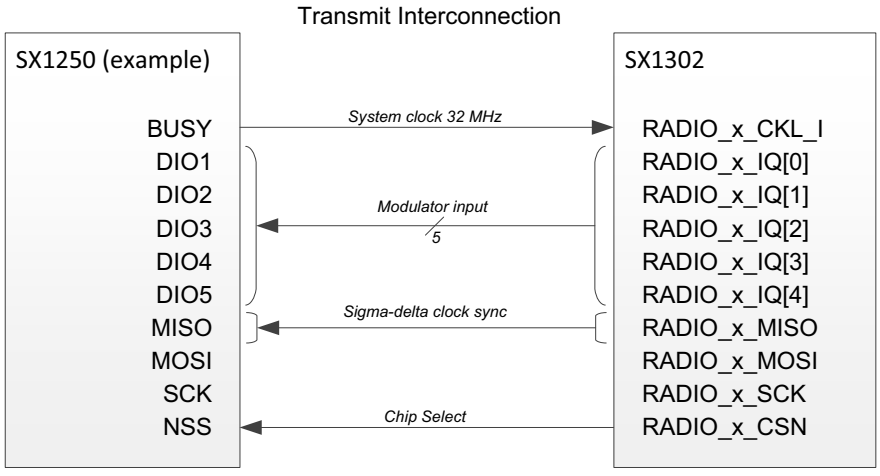


Figure 4-2: Transmit Interconnection

The table hereafter summarizes the characteristics of the three front-end devices currently supported with the SX1302:

Table 4-1: Semtech RF Front-end Summary

Part #	Frequency Band	Receive BW	Output Power	Rx NF	Comment
SX1255	400 - 510 MHz	1 MHz	About 0 dBm	5 dB	5x5 mm package, 20 mA Rx
SX1257	862 - 1020 MHz	1 MHz	About 0 dBm	5 dB	5x5 mm package, 20 mA Rx
SX1250	150 - 960 MHz	1 MHz	+22 dBm	10 dB	4x4 mm package, 5 mA Rx

5. Power Distribution

The SX1302 needs two powers rails: VCC_IO and VCC_CORE. VCC_IO sets the voltage level for all of the digital interfaces of the chip (SPI, GPIO and IQ interface), whilst VCC_CORE supplies current to the baseband engine. VCC_CORE can be derived from a higher voltage source with a high-efficiency DC-DC buck converter, as it is only 1.2 V. An optimized power management strategy is proposed in Semtech's reference designs, and one example of displayed in Section 10.2 "Reference Block Diagram" on page 24 .

The following currents can be measured, and should be used to design the power supply in the system:

Table 5-1: Current Consumption

	Conditions	VCC_CORE
	Temperature	**@ 1.2 V**
Average current	25°C	17 mA
Peak current	25°C	28 mA
Average current	60°C	48 mA
Peak current	60°C	55 mA
Average current	85°C	77 mA
Peak current	85°C	85 mA

During a reception phase, the current observed won't be always the same, but will spike up during certain phases of the reception. Therefore, the **average current** should be used to compute the total energy consumption of the SX1302 based gateway, however the **peak current** will be the relevant metric to size the power supply components.

To ensure proper control of all digital IOs during the power-up and power-down sequences of the SX1302, VCC_CORE shall be enabled *before* VCC_IO at start-up, and disabled *after* VCC_IO at shut-down.

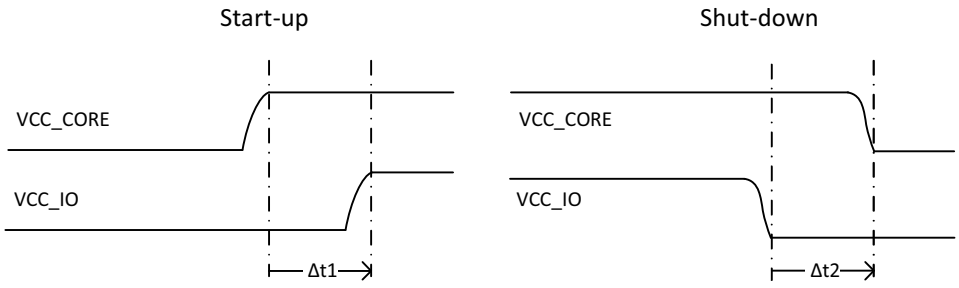


Figure 5-1: VCC_CORE and VCC_IO Sequencing

Δt1 and Δt2 must be equal to or greater than 0.

6. Clocking

The SX1302 uses the 32 MHz clock source from its companion RF Front-end (for example, Semtech's SX1250) to clock the entire system. This clock is injected on pin 43 (RADIO_A_CLK_I). It is advised to use a GPS-precision TCXO (0.5 ppm), in order to have a maximum "capture range" for the receiver, allowing lower precision reference clock, which are cheaper, on the end-devices.

7. Detection Engine - Modems

The SX1302 embeds 16 different modems, of two sorts:

- 8 multi-SF LoRa® modems, capable of demodulating any LoRa® packet from SF5 to SF12
- 8 multi-SF LoRa® modems, specifically demodulating SF5 to SF10 traffic
- 1 high-speed multi-BW LoRa® modem (125, 250 or 500 kHz), handling a single declared SF

A holistic detection engine can capture any LoRa® traffic in the pre-defined frequency plan, and assign the detected packets to the pool of available modems for demodulation.

8. Digital Interface and Control

The transceiver is controlled via a serial interface (SPI) and a set of general purpose input/output (DIOs).

8.1 Host SPI Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex frame corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature.

An address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The CSN pin goes low at the beginning of the frame and goes high after the data byte.

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer is always started by the CSN pin going low. MISO is high impedance when CSN is high.

The host terminates an SPI transaction by raising the CSN signal, it does not explicitly send the command length as a parameter. The host must not raise CSN within the bytes of a transaction.

8.1.1 HOST SPI Timings

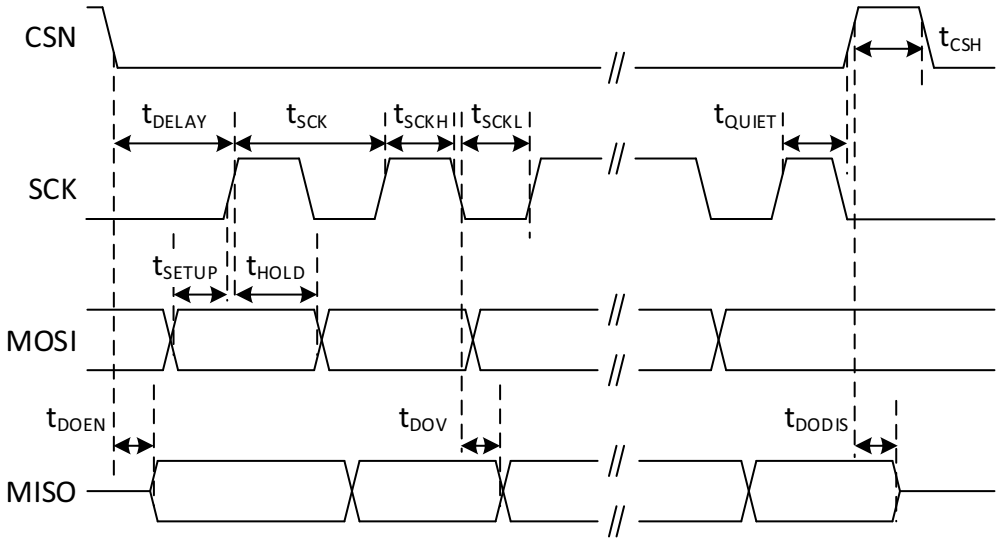


Figure 8-1: SPI Timing Diagram

8.1.2 SPI Timings

All timings are given in next table for Max load cap of 10 pF.

Table 8-1: SPI Timing Requirements

Symbol	Description	Minimum	Typical	Maximum	Unit
Timing constraints in SPI inputs					
$t_{SPI,SCK}$	SCK period	100			ns
$t_{SPI,SCKH}$	SCK high duration	40			ns
$t_{SPI,SCKL}$	SCK low duration	40			ns
$t_{SPI,SCKR}$	SCK rise time (10% VCC_IO ->90% VCC_IO)	0	2.5		ns
$t_{SPI,SCKF}$	SCK fall time (90% VCC_IO ->10% VCC_IO)	0	2.5		ns
$t_{SPI,DELAY}$	SCK lead time	40			ns
$t_{SPI,QUIET}$	SCK trail time	40			ns
$t_{SPI,CSH}$	Time between two successive CSN chip select	250			ns
$t_{SPI,CSR}$	CSN rise time (10% VCC_IO ->90% VCC_IO)	0	2.5		ns
$t_{SPI,CSF}$	CSN fall time (90% VCC_IO ->10% VCC_IO)	0	2.5		ns
$t_{SPI,SETUP}$	Data in setup time	5			ns
$t_{SPI,HOLD}$	Data in hold time	5			ns
SPI output timing specification					
$t_{SPI,DOEN}$	SPI output enable time	0		10	ns
$t_{SPI,DODIS}$	SPI output disable time	0		10	ns
$t_{SPI,DOV}$	SCK out falling edge to MISO delay			15	ns

9. Application Programming Interface

Through SPI interface, the SX1302 is fully controlled by its host, whether it is a MCU (smal-size cell) or a Linux MPU for higher-end gateways.

Semtech fully abstracts the complexity of the SX1302 and its companions chips by delivering two libraries as open-source code:

- SX1302 HAL (Hardware Abstraction layer), incorporating all of the required code to initialize, calibrate, run and exchange radio packets with the gateway board
- SX1302 Packet Forwarder, which is a simple example application of how a gateway can be connected to a host. The host, in a LoRaWAN network, is typically cloud-based, but can also be co-located with the gateway in case of small-scale networks

All of these open-sourced libraries are available from Github on https://github.com/Lora-net/sx1302_hal.

9.1 Globally Unique EUI

The SX1302 chip is serialized in production, with a globally unique 64-bit number. It may be used by the application for identification and security purposes.

This 64-bit EUI can be retrieved with the function *lgw_get_eui()* available in the HAL library.

10. Application Information

The Core cell reference design represents a compact reference implementation of the SX1302, along with its power management, clocks, Front End Module, RF matching and filtering.

10.1 Geographical Designs

The suitability of the SX1302-based reference designs to national radio frequency regulations depends on the RF front-end device being used. With the SX1250/55/57 front-ends provided by Semtech, the expectation is:

- Up to +27 dBm supported in the USA, Canada or other FCC-type countries
- Up the +27 dBm in Europe and other ITU 1 regions
- Up to +21 dBm in Japan where the phase noise requirement is more stringent

10.2 Reference Block Diagram

The application block diagram is shown below:

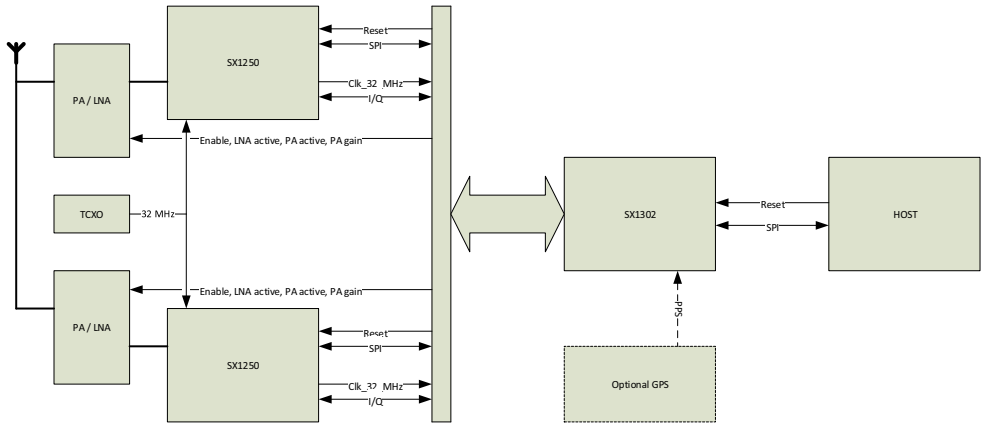


Figure 10-1: Application Design Block Diagram

10.3 Reference Design Layout

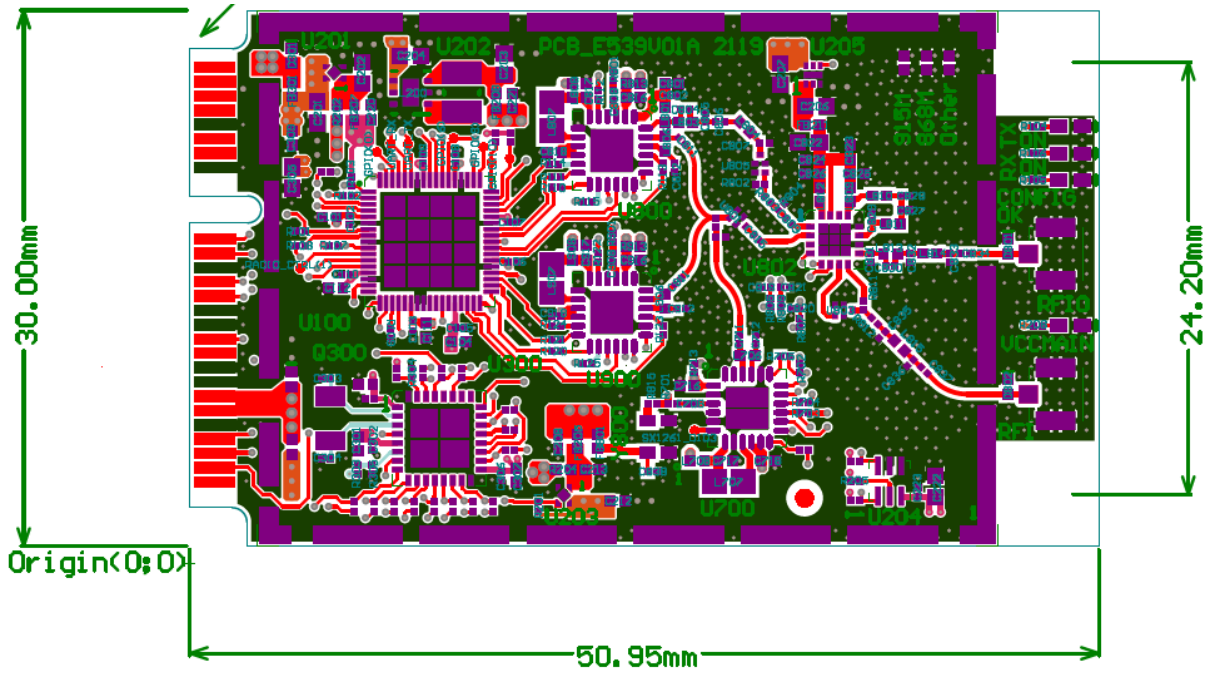
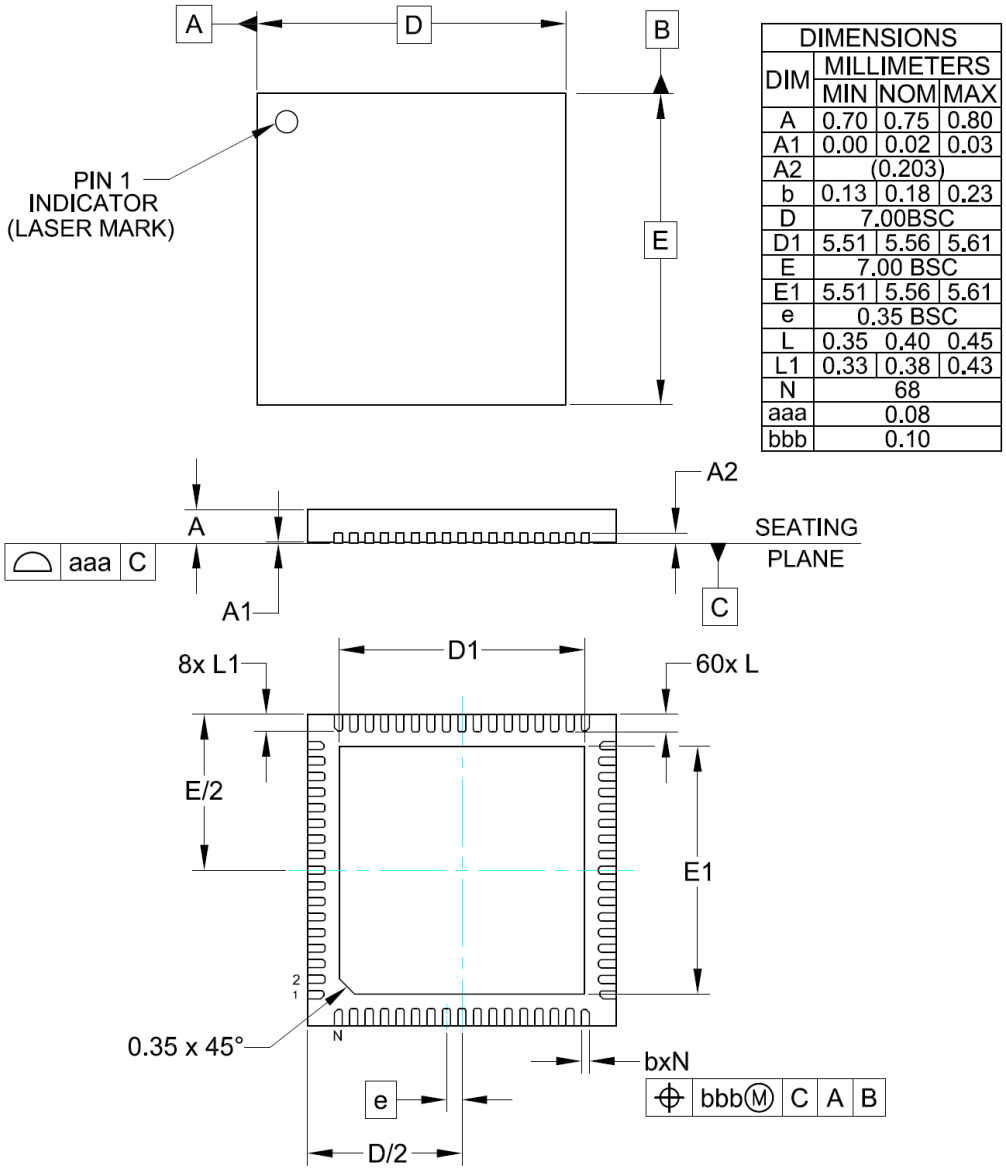


Figure 10-2: Reference Design PCB Layout

11. Packaging Information

11.1 Package Outline Drawing

The transceiver is delivered in a 7x7mm QFN package with 0.35mm pitch:



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.03
A2		(0.203)	
b	0.13	0.18	0.23
D		7.00BSC	
D1	5.51	5.56	5.61
E		7.00 BSC	
E1	5.51	5.56	5.61
e		0.35 BSC	
L	0.35	0.40	0.45
L1	0.33	0.38	0.43
N		68	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 11-1: QFN 7x7 Package Outline Drawing

11.2 Package Marking

TOP MARK	
CHAR	ROWS
7/7/7/7/7	5

Marking for the 7 x 7 mm MLPQ 68ld Lead package:

nnnnnn = Part Number (Example: SX1302)
yyww = Date Code (Example: 1852)
xxxxxxx = Semtech Lot No. (Example: EA90101)
xxxxxxx 0101-10)

Figure 11-2: SX1302 Package Marking

11.3 Land Pattern

The recommended land pattern is as follows:

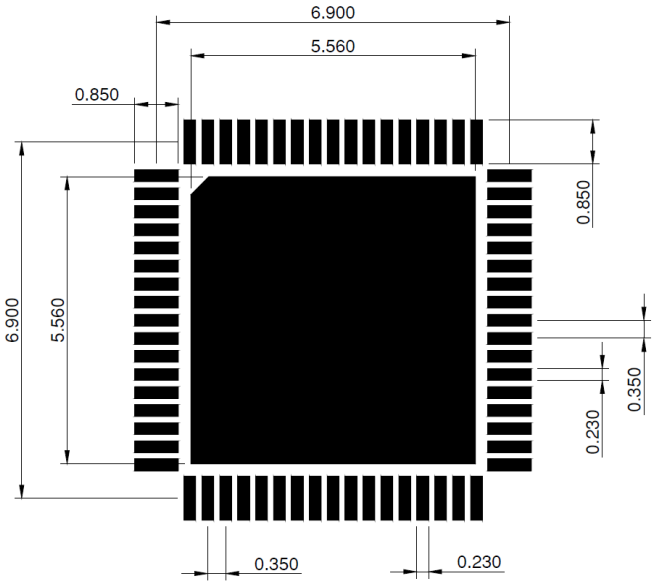


Figure 11-3: QFN 7x7mm Land Pattern

11.4 Reflow Profiles

Reflow process instructions are available from the Semtech website, at the following address:

http://www.semtech.com/quality/ir_reflow_profiles.html

The transceiver uses a QFN68 7x7mm package, also named MLP package.

11.5 Tape and Reel Specification

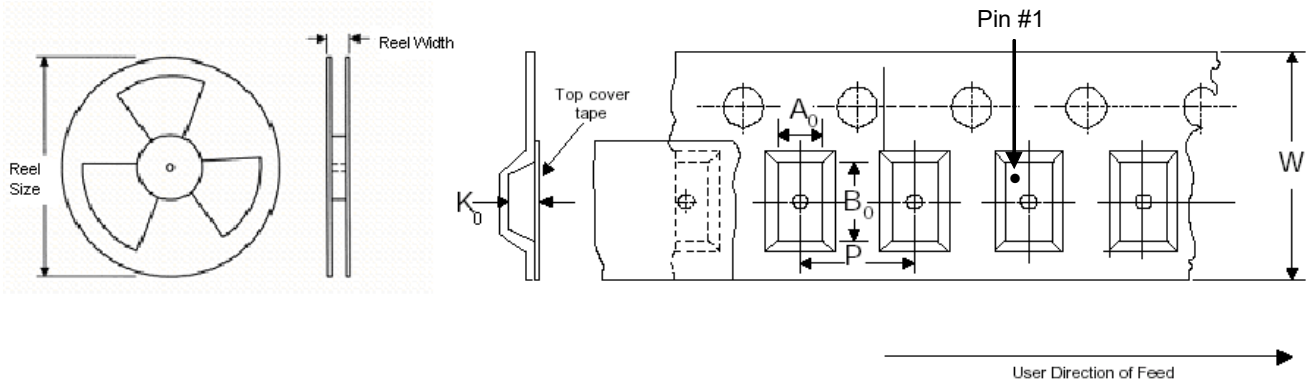


Figure 11-4: Tape and Reel Specification

Table 11-1: Tape and Reel Specification

Package Size	Carrier Tape (mm)					Reel				
	Tape Width[1] (W)	Pocket[2] Pitch (P)	A_O[3]	B_O	K_O[4]	Reel Size [in]	Reel Width [mm]	Min. Trailer Length [mm]	Min. Leader Length [mm]	QTY per Reel
7 x 7	16	12	7.3	7.3	1.1	13	16.4	400	400	3000

1. Tolerance for tape width is +/- 0.3 mm
2. Single Sprocket holes, pocket pitch range +/-0.1 mm
3. Range from nominal values for Ao and Bo is +/-0.2 mm
4. Range is +/-0.1 mm

11.6 Thermal Impedance

The thermal impedance of this package is:

- 28.3 °C/W when used in still air (natural convection)
- 21.6 °C/W when used with an air speed of 1 m/s
- 19.5 °C/W when used with an air speed of 2.5 m/s

This measurement is made with a 1.6 mm 4-layer PCB of 87 cm^2, metallized over 55 cm^2, with 16 vias of 0.3 mm diameter.

Glossary

List of Acronyms and their Meaning

Acronym	Meaning
ACR	Adjacent Channel Rejection
ADC	Analog-to-Digital Converter
AFC	Automatic Frequency Correction
AGC	Automatic Gain Control
API	Application Programming Interface
β	Modulation Index
BR	Bit Rate
BT	Bandwidth-Time bit period product
BW	BandWidth
CAD	Channel Activity Detection
CMD	Command Transaction
CPOL	Clock Polarity
CPHA	Clock Phase
CR	Coding Rate
CRC	Cyclical Redundancy Check
CSN	Chip Select active low
CW	Continuous Wave
DC-DC	Direct Current to Direct Current converter
DIO	Digital Input / Output
DSB	Double Side Band
FEC	Forward Error Correction
FLRC	Fast Long Range Communication
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
IF	Intermediate Frequencies
IRQ	Interrupt Request
LDO	Low-Dropout
LNA	Low-Noise Amplifier

List of Acronyms and their Meaning

Acronym	Meaning
LO	Local Oscillator
LoRa®	Long Range Communication *the LoRa® Mark is a registered trademark of the Semtech Corporation*
LSB	Least Significant Bit
MD	More Data
MIC	Message Integrity Check
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
MSK	Minimum-Shift Keying
NESN	Next Expected Sequence Number
NOP	No Operation
NRZ	Non-Return-to-Zero
OOK	On-Off Keying
PA	Power Amplifier
PDU	Protocol Data Unit
PER	Packet Error Rate
PID	Product Identification
PLL	Phase-Locked Loop
PRNG	Pseudo-Random Number Generation
RFU	Reserved for Future Use
RTC	Real-Time Clock
RTSN	Request to Send
SCK	Serial Clock
SF	Spreading Factor
SN	Sequence Number
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
STDBY	Standby
TCXO	Temperature Compensated Crystal Oscillator
UART	Universal Asynchronous Receiver/Transmitter
XOSC	Crystal Oscillator

Contact Information

Semtech Corporation
Wireless & Sensing Products
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com