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NTE74HCT240 & NTE74HCT244
Integrated Circuit
TTL – High Speed CMOS,
Octal Buffer/Line Driver/Receiver
with 3–State Outputs

Description:

The NTE74HCT240 (Inverting Outputs) and NTE74HCT244 (Non–Inverting Outputs) are 3–STATE buffers in a 20–Lead DIP type package that utilize advanced silicon–gate CMOS technology and are general purpose high speed buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS–TTL equivalent inputs. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers.

These devices are intended to interface between TTL and NMOS components and standard CMOS devices and are also plug–in replacements for LS–TTL devices and can be used to reduce power consumption in existing designs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and GND.

Features:

- TTL Input Compatible
- Typical Propagation Delay: 14ns
- 3–STATE Outputs for Connection to System Buses
- Low Quiescent Current: 80μA
- High Output rive Current: 6mA (min)

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±35mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±70mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2. Unless otherwise specified, all voltages are referenced to GND.
Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	5.5	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times	t_r, t_f	–	–	500	ns

DC Electrical Characteristics: (V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions		T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}			–	2.0	2.0	V
Maximum Low Level Input Voltage	V_{IL}			–	0.8	0.8	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\|$ = 20μA	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			$\|I_{OUT}\|$ = 6.0mA, V_{CC} = 4.5V	4.2	3.98	3.84	V
			$\|I_{OUT}\|$ = 7.2mA, V_{CC} = 5.5V	5.7	4.98	4.84	V
Maximum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	$\|I_{OUT}\|$ = 20μA	0	0.1	0.1	V
			$\|I_{OUT}\|$ = 6.0mA, V_{CC} = 4.5V	0.2	0.26	0.33	V
			$\|I_{OUT}\|$ = 7.2mA, V_{CC} = 5.5V	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		–	±0.05	±0.5	μA
Maximum 3–STATE Output Leakage Current	I_{OZ}	V_{OUT} = V_{CC} or GND, $\overline{G}$ = V_{IH}, G = V_{IL}		–	±0.25	±2.5	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		–	4.0	40	μA
		V_{IN} = 2.4V or 0.5V, Note 4		0.6	1.0	1.3	mA

Note 4. This is measured per input with all other inputs held at V_{CC} or GND.

AC Electrical Characteristics: (V_{CC} = 5V, t_r = t_f = 6ns, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Output Propagation Delay	t_{PHL}, t_{PLH}	C_L = 45pF	14	18	ns
Maximum Output Enable Time	t_{PZL}, t_{PZH}	C_L = 45pF, R_L = 1kΩ	20	30	ns
Maximum Output Disable Time	t_{PLZ}, t_{PHZ}	C_L = 5pF, R_L = 1kΩ	16	25	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, t_r = t_f = 6ns unless otherwise specified)

Parameter	Symbol	Test Conditions		T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Maximum Output Propagation Delay	t_{PHL}, t_{PLH}	C_L = 50pF		14	20	25	ns
		C_L = 150pF		20	28	35	ns
Maximum Output Enable Time	t_{PZH}, t_{PZL}	R_L = 1kΩ	C_L = 50pF	21	30	38	ns
			C_L = 150pF	26	42	53	ns
Maximum Output Disable Time	t_{PHZ}, t_{PLZ}	R_L = 1kΩ, C_L = 50pF		16	25	32	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}	C_L = 50pF		6	12	15	ns
Maximum Input Capacitance	C_{IN}			10	15	15	pF
Maximum Output Capacitance	C_{OUT}			15	20	20	pF
Power Dissipation Capacitance (Per Buffer, Note 5)	C_{PD}	$\overline{G}$ = V_{CC}, G = GND		5	–	–	pF
		$\overline{G}$ = GND, G = V_{CC}		90	–	–	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Tables:

NTE74HCT240:

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

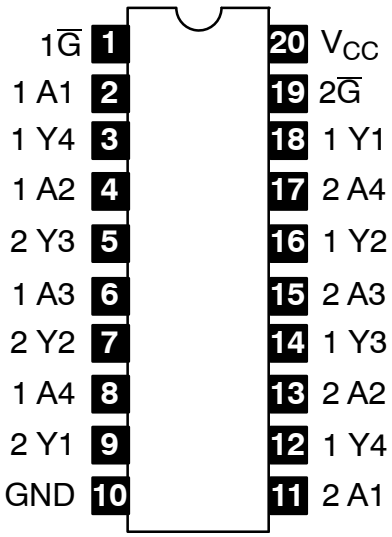
H = HIGH Level
L = LOW Level
Z = High Impedance

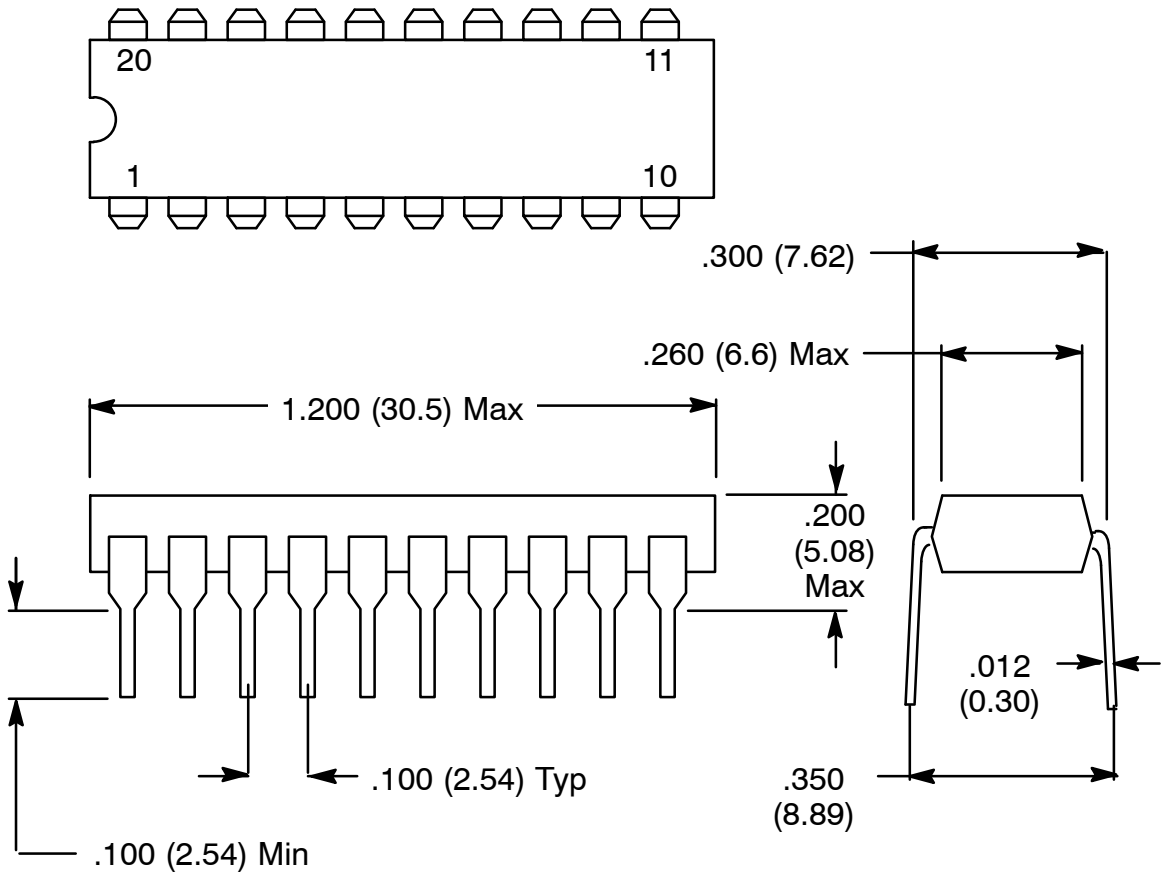
NTE74HCT244:

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = HIGH Level
L = LOW Level
Z = High Impedance

Pin Connection Diagram




20
11
1
10
.300 (7.62)
.260 (6.6) Max
1.200 (30.5) Max
.200
(5.08)
Max
.012
(0.30)
.100 (2.54) Typ
.350
(8.89)
.100 (2.54) Min